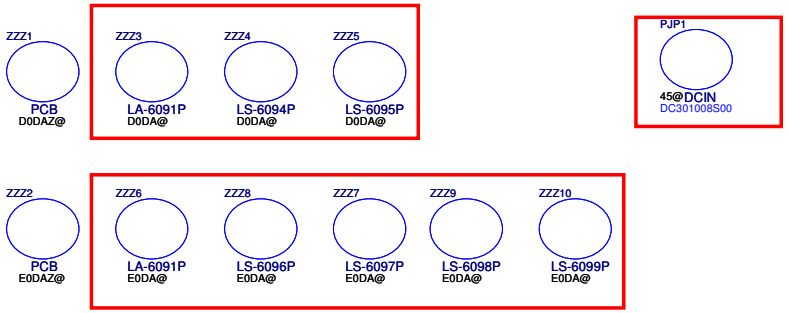

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NAVD0 Schematics Document

Intel Pineview Processor with Tigerpoint + DDRII + NV OPTIMUS

2010-02-09

REV: 1.0

Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

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Title: Cover Page		
Size: B	Document Number: NAVD0 LA-6091P	Rev: 1.0
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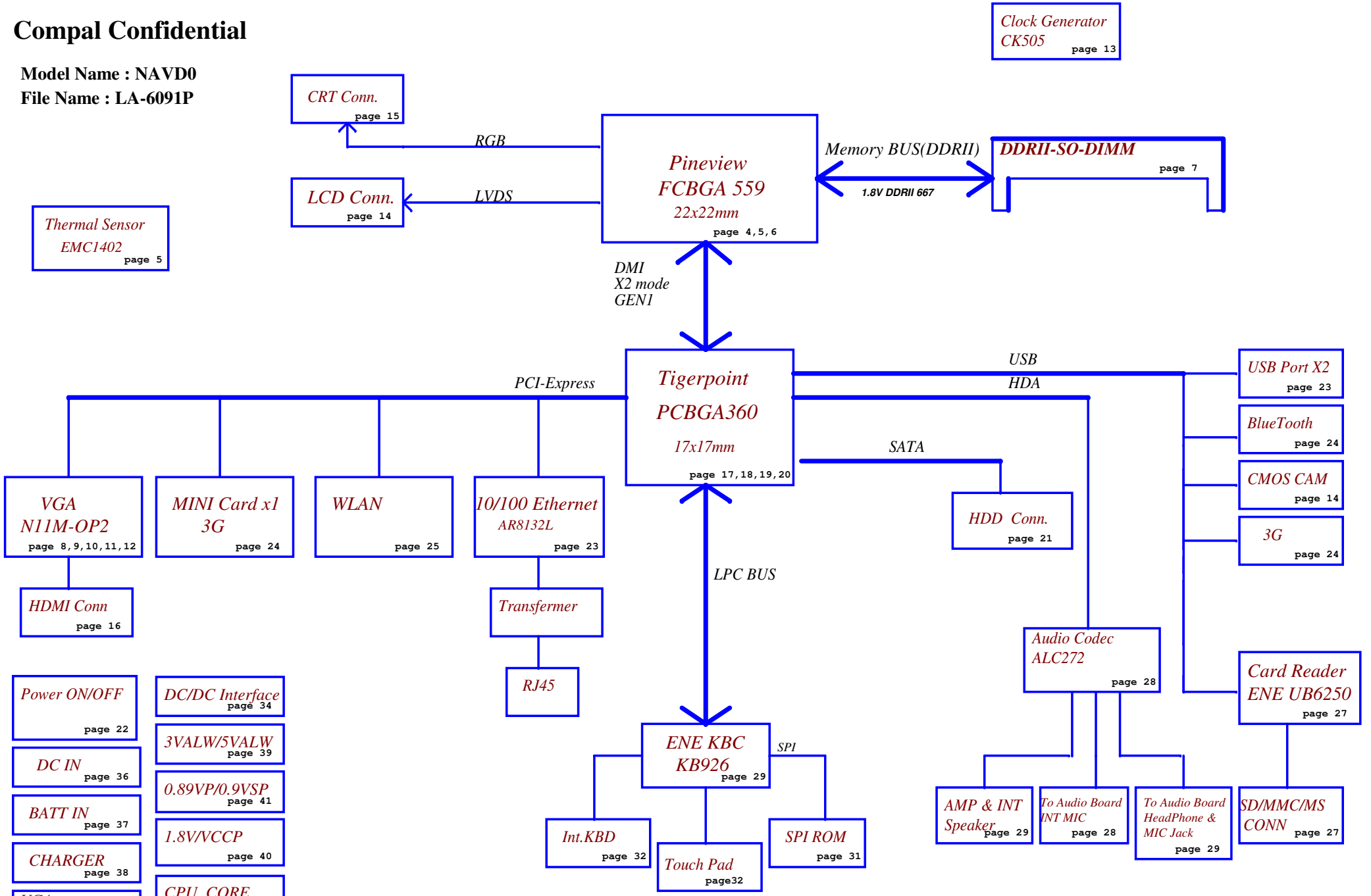
Model Name : NAVD0
File Name : LA-6091P



Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

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Title	Block Diagrams	
Size B	Document Number NAVD0 LA-6091P	Rev 1.0
Date: Wednesday, March 03, 2010	Sheet 2 of 46	

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+0.89VS	Graphic core power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table(Page 31)

	VCC	3.3V				
	Ra	100K				
	ID	BRD ID	Rb	Vab-Min	Vab-Typ	Vab-Max
NAVD0	0	R01 (EVT)	0	0V	0V	0V
	1	R02 (DVT)	8.2K	0.216V	0.250V	0.289V
	2	R03 (PVT)	18K	0.436V	0.503V	0.538V
	3	R10A (MP)	33K	0.712V	0.819V	0.875V
NAVE0	4	R01 (EVT)	56K	1.036V	1.185V	1.264V
	5	R02 (DVT)	100K	1.453V	1.650V	1.759V
	6	R03 (PVT)	200K	1.935V	2.200V	2.341V
	7	R10A (MP)	NC	2.500V	3.3V	3.3V

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ

No PCI Device

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
EMC1402	100_1100

ICH7M SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb

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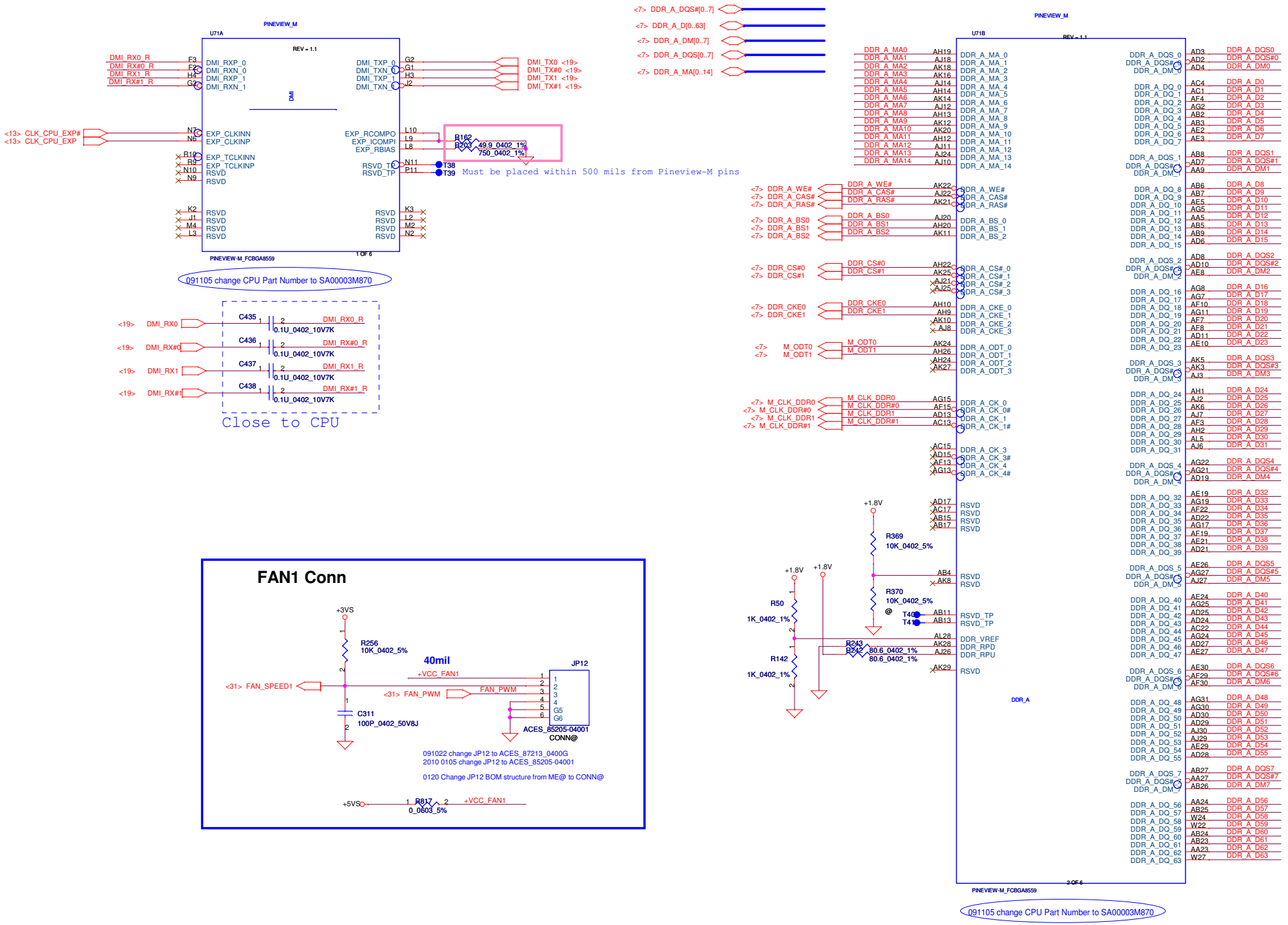
Title: Notes List

Size: B | Document Number: NAVD0 LA-6091P | Rev: 1.0

Date: Wednesday, March 03, 2010 | Sheet 3 of 46



Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

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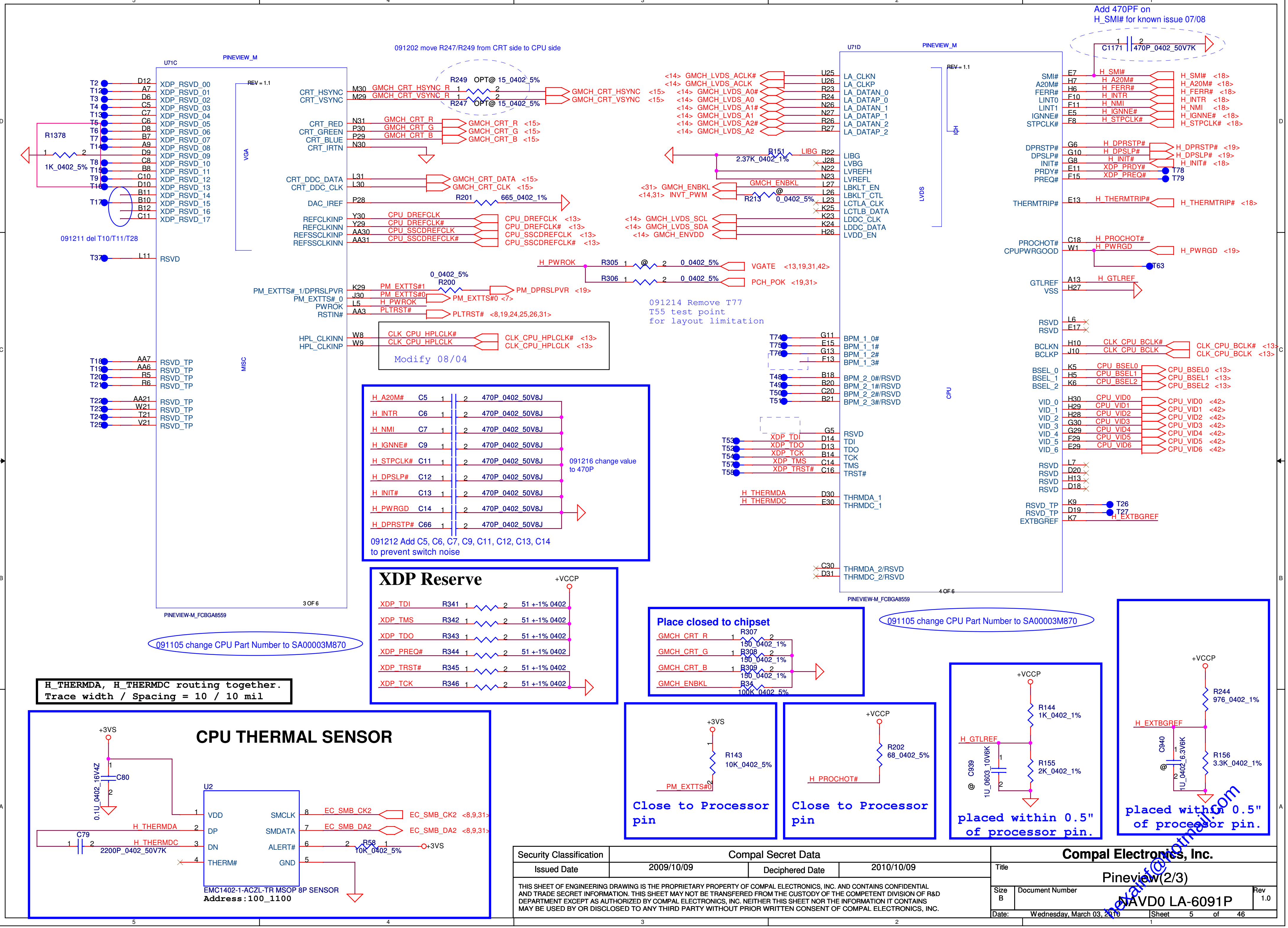
Title: Pineview(1/3)

Size	Document Number	Rev
Custom	NAVD0 LA-6091P	1.0

Date: Wednesday, March 03, 2010 | Sheet 4 of 46



Add 470PF on
H_SMI# for known issue 07/08
091202 move R247/R249 from CRT side to CPU side
U71C
PINEVIEW_M
XDP_RSVD_00
XDP_RSVD_01
XDP_RSVD_02
XDP_RSVD_03
XDP_RSVD_04
XDP_RSVD_05
XDP_RSVD_06
XDP_RSVD_07
XDP_RSVD_08
XDP_RSVD_09
XDP_RSVD_10
XDP_RSVD_11
XDP_RSVD_12
XDP_RSVD_13
XDP_RSVD_14
XDP_RSVD_15
XDP_RSVD_16
XDP_RSVD_17
R1378
1K_0402_5%
091211 del T10/T11/T28
RSVD
CRT_HSYNC
CRT_VSYNC
CRT_RED
CRT_GREEN
CRT_BLUE
CRT_IRTN
CRT_DDC_DATA
CRT_DDC_CLK
DAC_IREF
REFCLKINP
REFCLKINN
REFSSCLKINP
REFSSCLKINN
PM_EXTTS#_1/DPRSLPVR
PM_EXTTS#_0
PWROK
RSTIN#
HPL_CLKINN
HPL_CLKINP
RSVD_TP
VGA
MISC
3 OF 6
PINEVIEW-M_FCBGA8559
GMCH_CRT_HSYNC_R
GMCH_CRT_VSYNC_R
R249 OPT@ 15_0402_5%
R247 OPT@ 15_0402_5%
GMCH_CRT_HSYNC <15>
GMCH_CRT_VSYNC <15>
GMCH_CRT_R <15>
GMCH_CRT_G <15>
GMCH_CRT_B <15>
GMCH_CRT_DATA <15>
GMCH_CRT_CLK <15>
R201 665_0402_1%
CPU_DREFCLK <13>
CPU_DREFCLK# <13>
CPU_SSCDREFCLK <13>
CPU_SSCDREFCLK# <13>
R200 0_0402_5%
PM_DPRSLPVR <19>
PM_EXTTS#0 <7>
PLTRST# <8,19,24,25,26,31>
CLK_CPU_HPLCLK# <13>
CLK_CPU_HPLCLK <13>
Modify 08/04
H_PWROK
R305 @ 0_0402_5% VGATE <13,19,31,42>
R306 0_0402_5% PCH_POK <19,31>
091214 Remove T77
T55 test point
for layout limitation
GMCH_LVDS_ACLK#
GMCH_LVDS_ACLK
GMCH_LVDS_A0#
GMCH_LVDS_A0
GMCH_LVDS_A1#
GMCH_LVDS_A1
GMCH_LVDS_A2#
GMCH_LVDS_A2
R151 2.37K_0402_1%
LIBG
<31> GMCH_ENBKL
<14,31> INVT_PWM
R213 @ 0_0402_5%
<14> GMCH_LVDS_SCL
<14> GMCH_LVDS_SDA
<14> GMCH_ENVDD
U71D
PINEVIEW_M
LA_CLKN
LA_CLKP
LA_DATAN_0
LA_DATAP_0
LA_DATAN_1
LA_DATAP_1
LA_DATAN_2
LA_DATAP_2
LIBG
LVBG
LVREFH
LVREFL
LBKLT_EN
LBKLT_CTL
LCTLA_CLK
LCTLB_DATA
LDDC_CLK
LDDC_DATA
LVDD_EN
LVDS
BPM_1_0#
BPM_1_1#
BPM_1_2#
BPM_1_3#
BPM_2_0#/RSVD
BPM_2_1#/RSVD
BPM_2_2#/RSVD
BPM_2_3#/RSVD
RSVD
TDI
TDO
TCK
TMS
TRST#
XDP_TDI
XDP_TDO
XDP_TCK
XDP_TMS
XDP_TRST#
H_THERMDA
H_THERMDC
THRMDA_1
THRMDC_1
THRMDA_2/RSVD
THRMDC_2/RSVD
4 OF 6
PINEVIEW-M_FCBGA8559
CPU
SMI#
A20M#
FERR#
LINT0
LINT1
IGNNE#
STPCLK#
DPRSTP#
DPSLP#
INIT#
PRDY#
PREQ#
THERMTRIP#
PROCHOT#
CPUPWRGOOD
GTLREF
VSS
BCLKN
BCLKP
BSEL_0
BSEL_1
BSEL_2
VID_0
VID_1
VID_2
VID_3
VID_4
VID_5
VID_6
RSVD_TP
EXTBGREF
C1171 470P_0402_50V7K
H_SMI# <18>
H_A20M# <18>
H_FERR# <18>
H_INTR <18>
H_NMI <18>
H_IGNNE# <18>
H_STPCLK# <18>
H_DPRSTP# <19>
H_DPSLP# <19>
H_INIT# <18>
XDP_PRDY#
XDP_PREQ#
H_THERMTRIP# <18>
H_PWRGD <19>
H_GTLREF
CLK_CPU_BCLK# <13>
CLK_CPU_BCLK <13>
CPU_BSEL0 <13>
CPU_BSEL1 <13>
CPU_BSEL2 <13>
CPU_VID0 <42>
CPU_VID1 <42>
CPU_VID2 <42>
CPU_VID3 <42>
CPU_VID4 <42>
CPU_VID5 <42>
CPU_VID6 <42>
H_EXTBGREF
H_A20M# C5 470P_0402_50V8J
H_INTR C6 470P_0402_50V8J
H_NMI C7 470P_0402_50V8J
H_IGNNE# C9 470P_0402_50V8J
H_STPCLK# C11 470P_0402_50V8J
H_DPSLP# C12 470P_0402_50V8J
H_INIT# C13 470P_0402_50V8J
H_PWRGD C14 470P_0402_50V8J
H_DPRSTP# C66 470P_0402_50V8J
091216 change value to 470P
091212 Add C5, C6, C7, C9, C11, C12, C13, C14
to prevent switch noise
XDP Reserve
+VCCP
XDP_TDI R341 51 +-1% 0402
XDP_TMS R342 51 +-1% 0402
XDP_TDO R343 51 +-1% 0402
XDP_PREQ# R344 51 +-1% 0402
XDP_TRST# R345 51 +-1% 0402
XDP_TCK R346 51 +-1% 0402
Place closed to chipset
GMCH_CRT_R R307 150_0402_1%
GMCH_CRT_G R308 150_0402_1%
GMCH_CRT_B R309 150_0402_1%
GMCH_ENBKL R34 100K_0402_5%
091105 change CPU Part Number to SA00003M870
091105 change CPU Part Number to SA00003M870
H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil
CPU THERMAL SENSOR
+3VS
C80 0.1U_0402_16V4Z
C79 2200P_0402_50V7K
U2
VDD
DP
DN
THERM#
SMCLK
SMDATA
ALERT#
GND
EC_SMB_CK2 <8,9,31>
EC_SMB_DA2 <8,9,31>
R58 10K_0402_5%
EMC1402-1-ACZL-TR MSOP 8P SENSOR
Address:100_1100
+3VS
R143 10K_0402_5%
PM_EXTTS#0
Close to Processor pin
+VCCP
R202 68_0402_5%
H_PROCHOT#
Close to Processor pin
+VCCP
R144 1K_0402_1%
R155 2K_0402_1%
C939 1U_0603_10V6K
H_GTLREF
placed within 0.5" of processor pin.
+VCCP
R244 976_0402_1%
R156 3.3K_0402_1%
C940 1U_0402_6.3V6K
H_EXTBGREF
placed within 0.5" of processor pin.

Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

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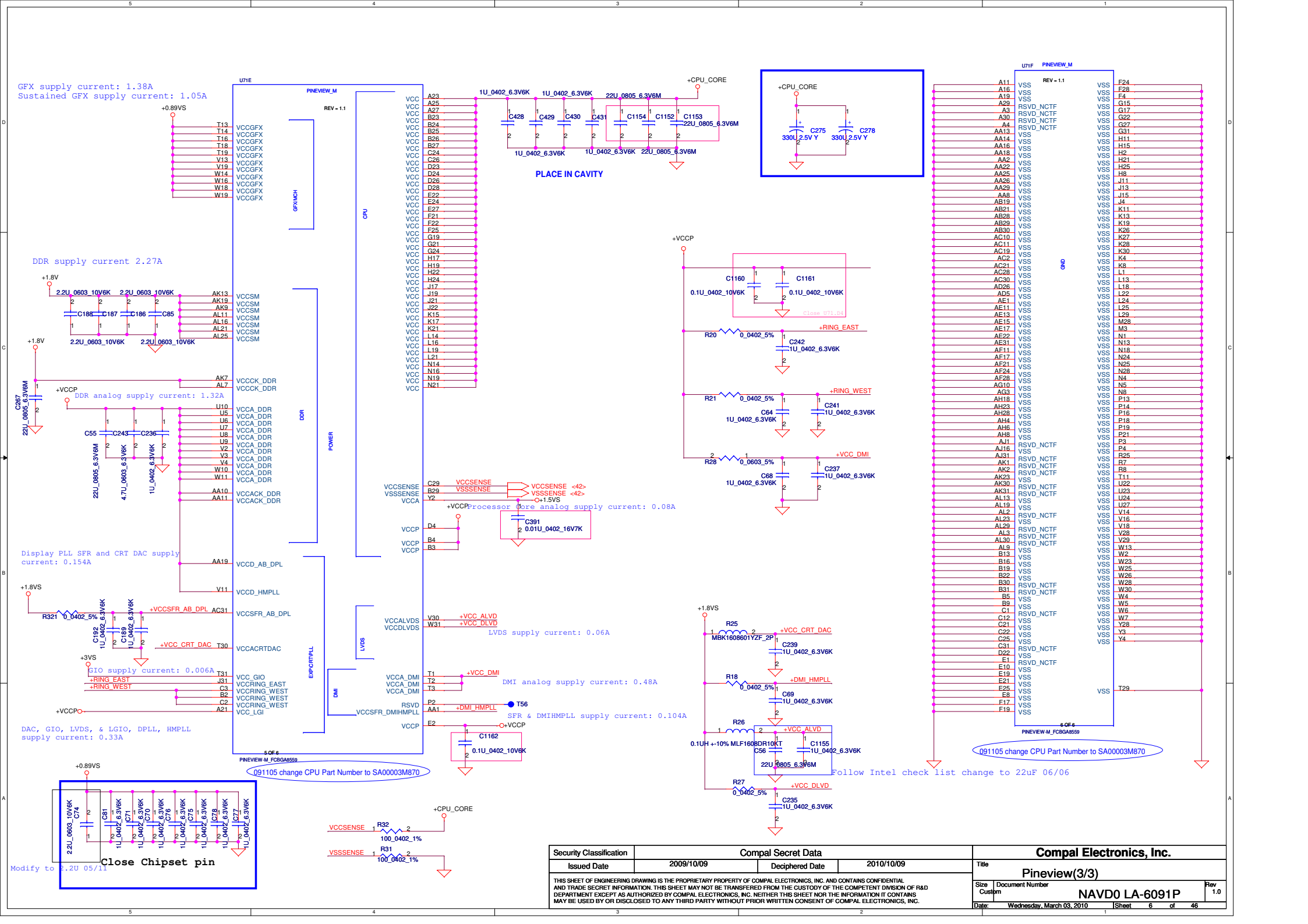
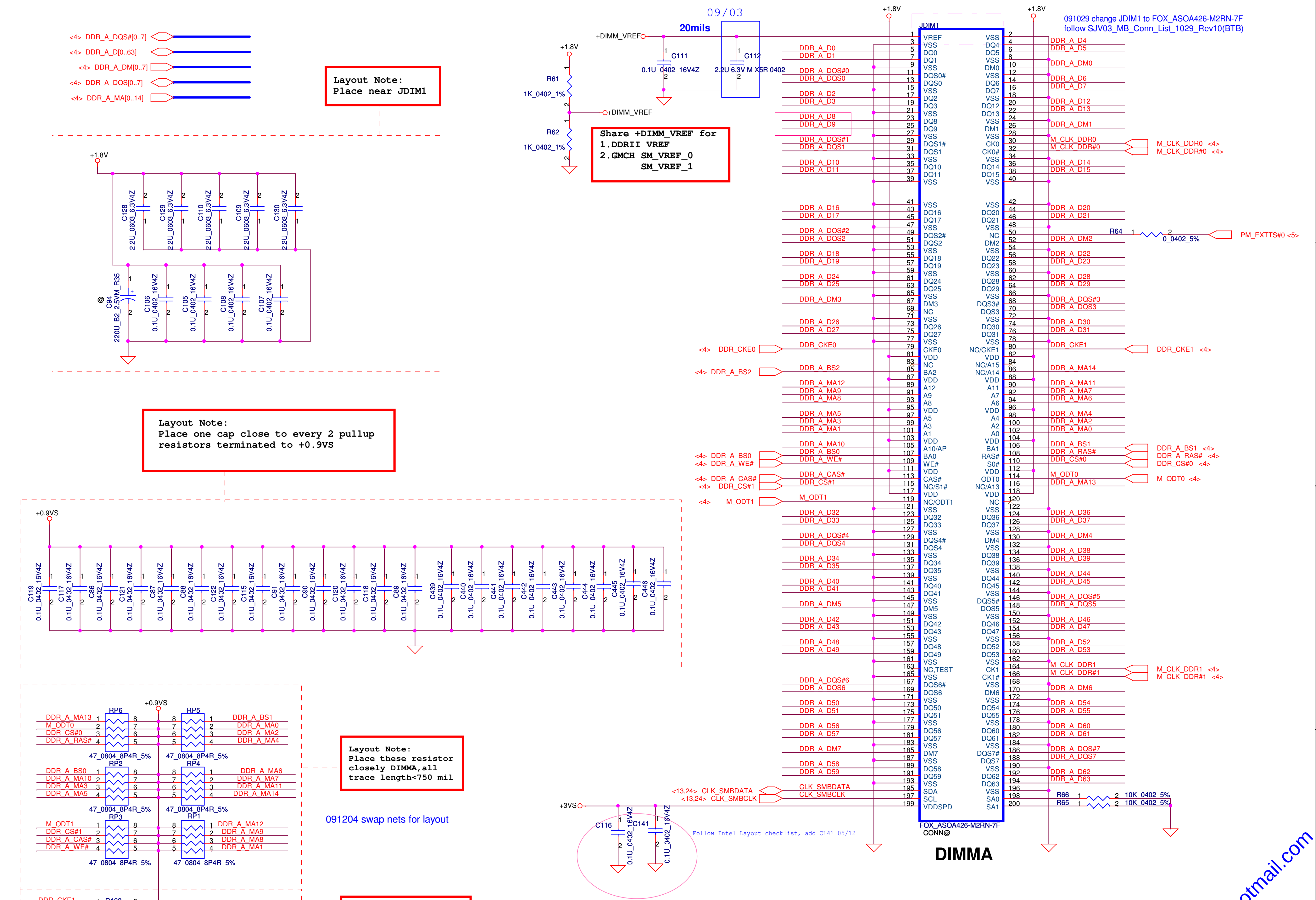
Title	Pineview(2/3)	
Size B	Document Number NAVD0 LA-6091P	Rev 1.0
Date: Wednesday, March 03, 2010	Sheet 5 of 46	


GFX supply current: 1.38A
Sustained GFX supply current: 1.05A
DDR supply current 2.27A
DDR analog supply current: 1.32A
Display PLL SFR and CRT DAC supply current: 0.154A
GIO supply current: 0.006A
DAC, GIO, LVDS, & LGIO, DPLL, HMPLL supply current: 0.33A
Processor core analog supply current: 0.08A
LVDS supply current: 0.06A
DMI analog supply current: 0.48A
SFR & DMIHMPLL supply current: 0.104A
PLACE IN CAVITY
Close Chipset pin
Modify to 2.2U 05/11
091105 change CPU Part Number to SA00003M870
Follow Intel check list change to 22uF 06/06
U71E PINEVIEW_M REV = 1.1
U71F PINEVIEW_M REV = 1.1
Compal Electronics, Inc.
Pineview(3/3)
NAVD0 LA-6091P
Compal Secret Data
2009/10/09
2010/10/09
Wednesday, March 03, 2010



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Issued Date	2009/10/09	Deciphered Date	2010/10/09

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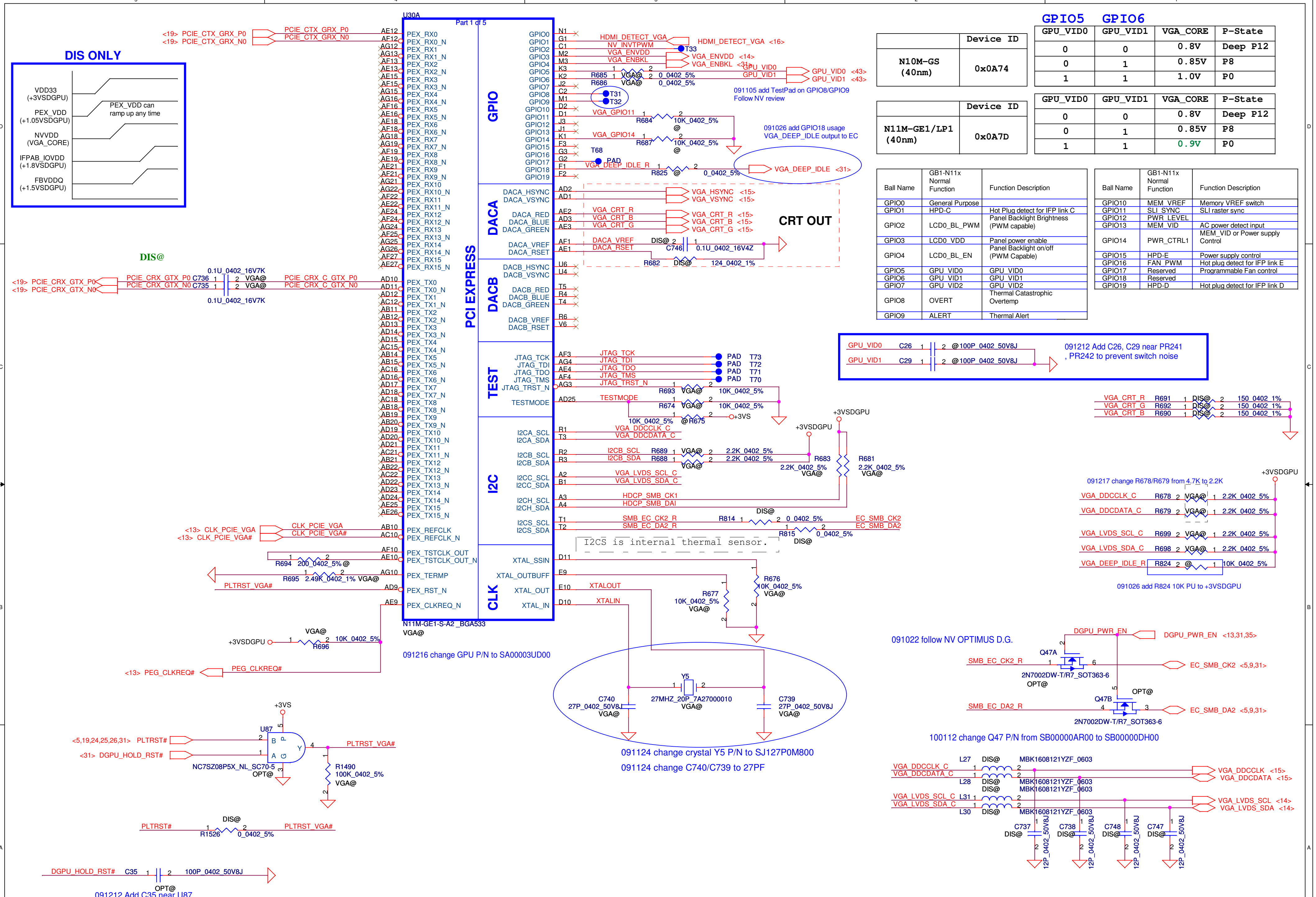
Title: DDRII-SODIMMA

Size: B | Document Number: NAWD0 LA-6091P | Rev: 1.0

Date: Wednesday, March 03, 2010 | Sheet 7 of 46



GPIO5 GPIO6

	Device ID
N10M-GS (40nm)	0x0A74

GPU_VID0	GPU_VID1	VGA_CORE	P-State
0	0	0.8V	Deep P12
0	1	0.85V	P8
1	1	1.0V	P0

	Device ID
N11M-GE1/LP1 (40nm)	0x0A7D

GPU_VID0	GPU_VID1	VGA_CORE	P-State
0	0	0.8V	Deep P12
0	1	0.85V	P8
1	1	0.9V	P0

Ball Name	GB1-N11x Normal Function	Function Description
GPIO0	General Purpose	
GPIO1	HPD-C	Hot Plug detect for IFP link C
GPIO2	LCD0_BL_PWM	Panel Backlight Brightness (PWM capable)
GPIO3	LCD0_VDD	Panel power enable
GPIO4	LCD0_BL_EN	Panel Backlight on/off (PWM Capable)
GPIO5	GPU_VID0	GPU_VID0
GPIO6	GPU_VID1	GPU_VID1
GPIO7	GPU_VID2	GPU_VID2
GPIO8	OVERT	Thermal Catastrophic Overtemp
GPIO9	ALERT	Thermal Alert

Ball Name	GB1-N11x Normal Function	Function Description
GPIO10	MEM_VREF	Memory VREF switch
GPIO11	SLI_SYNC	SLI raster sync
GPIO12	PWR_LEVEL	AC power detect input
GPIO13	MEM_VID	
GPIO14	PWR_CTRL1	MEM_VID or Power supply Control
GPIO15	HPD-E	Power supply control
GPIO16	FAN_PWM	Hot plug detect for IFP link E
GPIO17	Reserved	Programmable Fan control
GPIO18	Reserved	
GPIO19	HPD-D	Hot plug detect for IFP link D

Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

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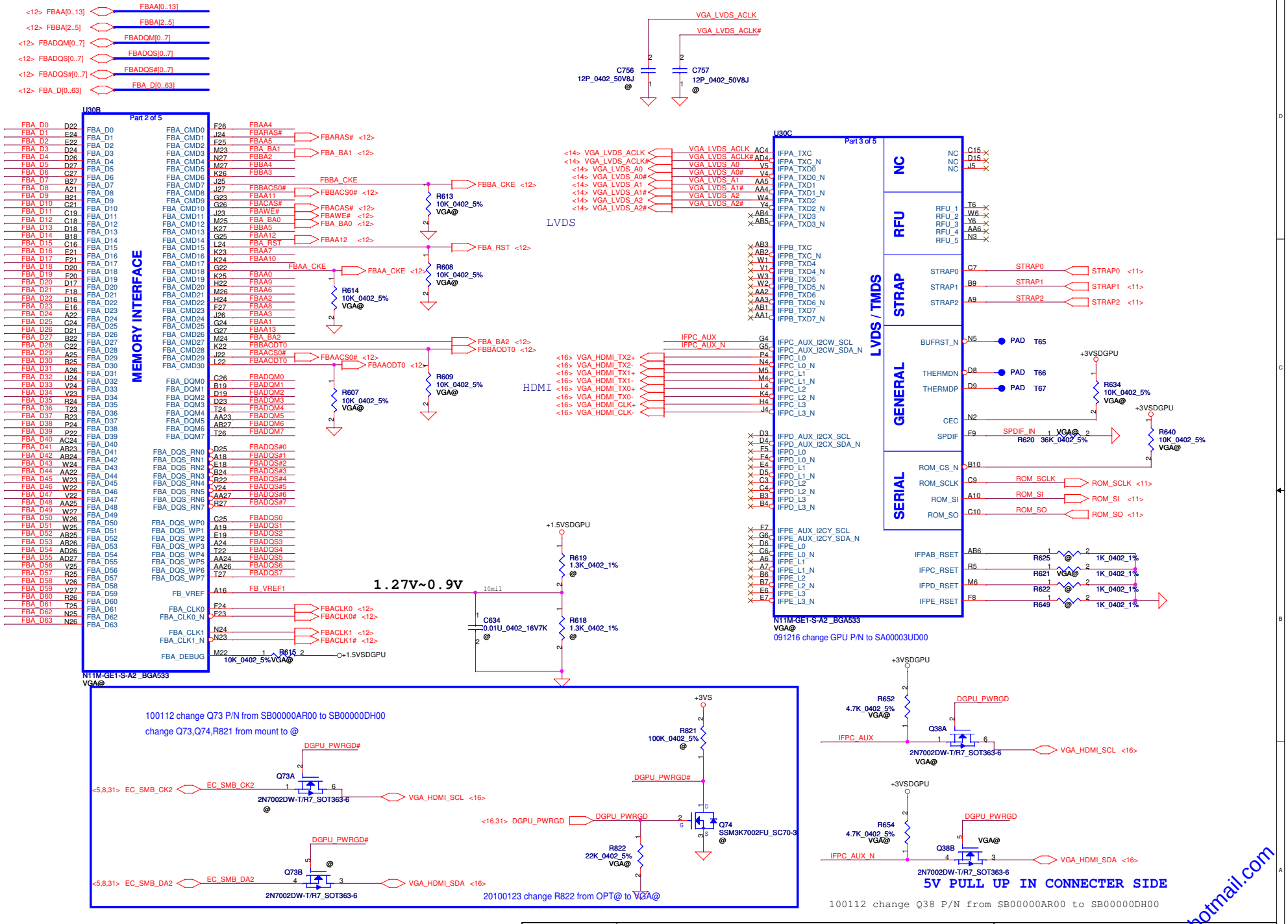
Title: N11M-OP2 PCIE,GPIO,CLK

Size: B — Document Number: NAVD0 LA-6091P — Rev 1.0



Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

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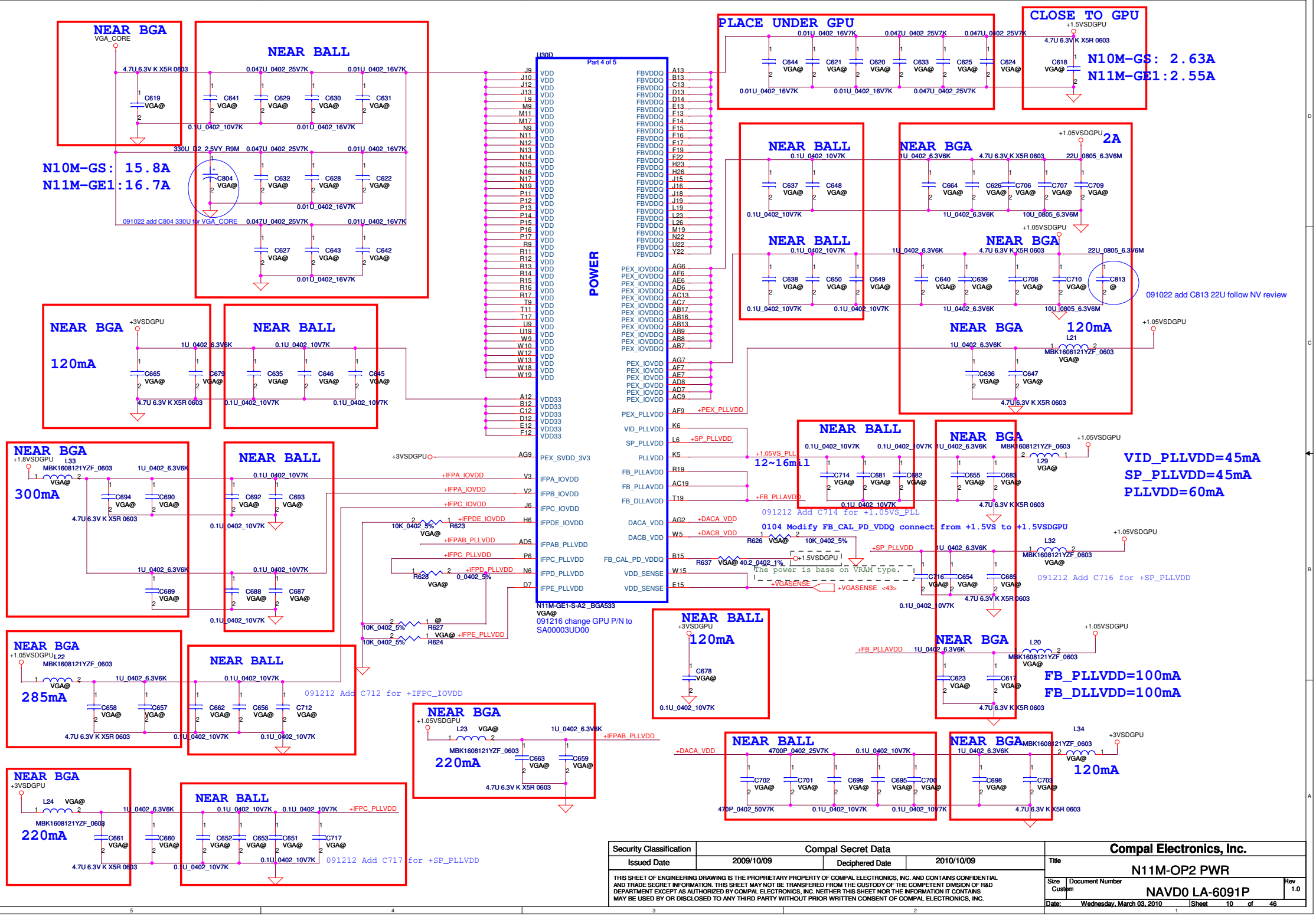
Title: N11M-OP2 LVDS Memory Bus

Size	Document Number	Rev
B	NAVD0 LA-6091P	1.0

Date: Wednesday, March 03, 2010 | Sheet 9 of 46



Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

Compal Electronics, Inc.

Title: N11M-OP2 PWR

Size: Custom | Document Number: NAVD0 LA-6091P | Rev: 1.0

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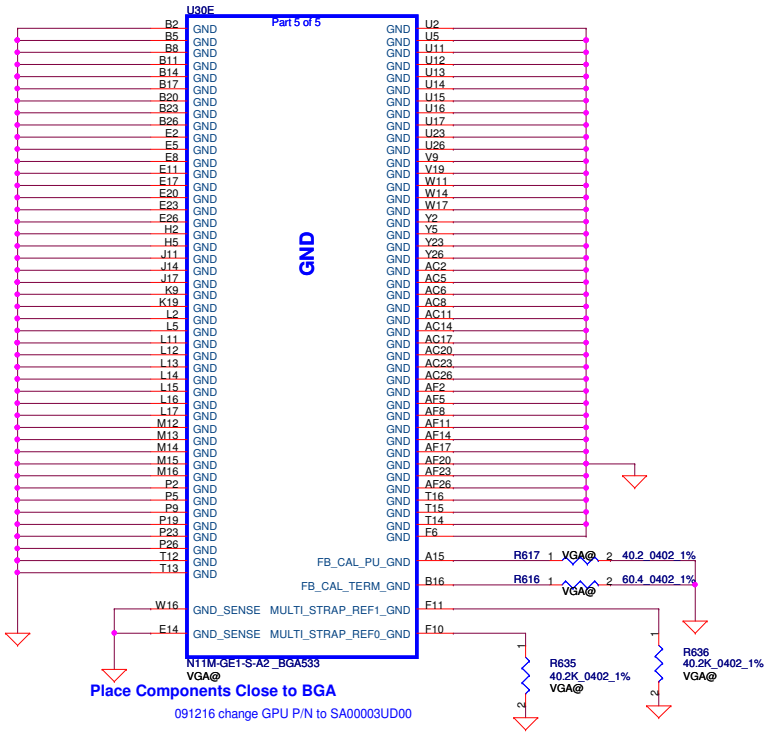
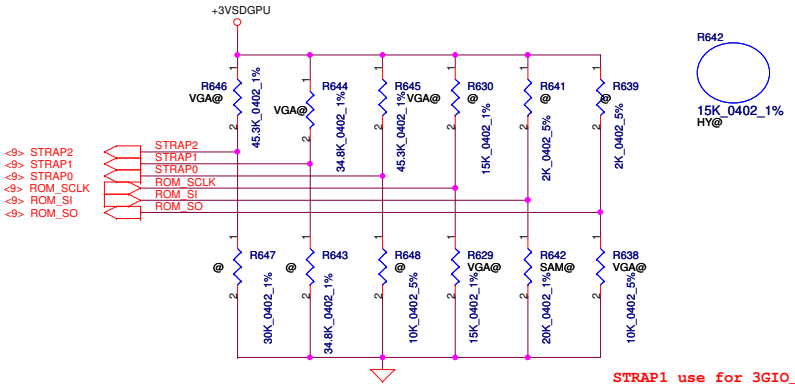
A total of 8 signals are required for GB1 strapping this includes
2 reference signals
6 physical strapping pins
4 logical strapping bits
A total of 24 logical strapping bits are available



Place Components Close to BGA

091216 change GPU P/N to SA00003UD00



STRAP1 use for 3GIO_PADCFG to set 35K pull up.
(PUN-04335-001_V10 HW9 update)

GPU	FB Memory (DDR3)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N11M-GE1 LP1 (0x0A7D) 40nm	Samsung 800MHz (defaul)	K4W1G1646E-HC12						
		64Mx16	PD 10K	PD 15K	PD 20K	PU 45K	PU 35K	PU 45K
	Hynix 800MHz	H5TQ1G63BFR-12C						
		64Mx16	PD 10K	PD 15K	PD 15K	PU 45K	PU 35K	PU 45K
					X76			

Resistor Values	Pull-up to VDD	Pull-down to GND
5Kohm	1000	0000
10Kohm	1001	0001
15Kohm	1010	0010
20Kohm	1011	0011
25Kohm	1100	0100
30Kohm	1101	0101
35Kohm	1110	0110
45Kohm	1111	0111

SUB_VENDOR	
0 *	No VBIOS ROM (Default)
1	BIOS ROM is present

XCLK_417	
0 *	277MHz (Default)
1	Reserved

Panel USER Straps	
User[3:0]	
EDID used *	Customer defined

SMBUS_ALT_ADDR	
0 *	0x9E (Default)
1	0x9C (Multi-GPU usage)

FB_0_BAR_SIZE	
0 *	256MB (Default)
1	Reserved

VGA_DEVICE	
0	3D Device
1 *	VGA Device (Default)

PEX_PLL_EN_TERM	
0 *	Disable (Default)
1	Enable

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110 *	Notebook Default

SLOT_CLOCK_CFG	
0 *	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

Physical Strapping Pin	Power Rail	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SO	VDD33	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	VDD33	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	VDD33	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	VDD33	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	VDD33	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	VDD33	USER[3]	USER[2]	USER[1]	USER[0]

	Memory/PKG	FBVDDQ	FB_CAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
N11M-GE1 LP1	DDR3	+1.5VS	40.2 ohm	40.2 ohm	40.2/60.4 ohm

Must be used 1% resister for driver calibration

DG-04642-001-V01(May 22, 2009)

Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

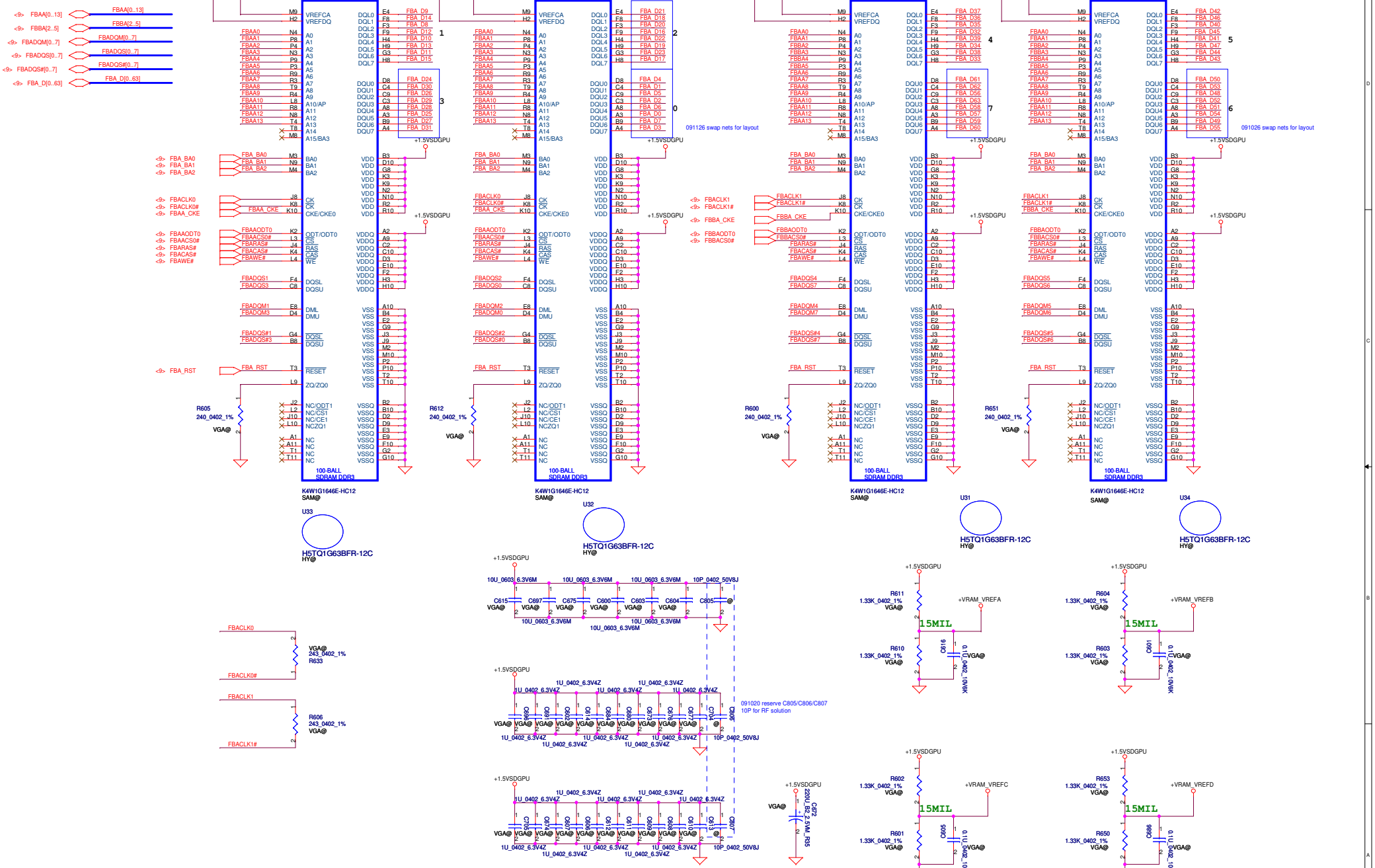
Compal Electronics, Inc.

Title: N11M-OP2 GND & STRAP

Size: B | Document Number: NAVD0 LA-6091P | Rev: 1.0

Date: Wednesday, March 03, 2010 | Sheet 11 of 46

N10x 40nm DDR3 MAPPING
NVIDIA COCUMENT FOR DA-3978-001



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Issued Date	2009/10/09	Deciphered Date	2010/10/09

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Compal Electronics, Inc.

Title: N11M-OP2 VRAM DDR3

Size	Document Number	Rev
C	NAVD0 LA-6091P	1.0

Date: Wednesday, March 03, 2010 Sheet 12 of 46

FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

Change C174 C175 to 10U_0603 05/14

Add C1145 C1146 C1147 for EMI 06/12

091212 Add C15 C16 near Q10 to prevent switch noise

100112 change Q47 P/N from SB00000AR00 to SB00000DH00

SA000020K00 (Silego : SLG8SP556VTR)
SA000020H10 (ICS : ICS9LPRS387AKLFT)

Change co-lay net name to +1.5VM_CK505 07/03

0301Change R1349,R1351 BOM structure from LOW_CLK@ to mount
0301Change R1348,R1350 BOM structure from NOR_CLK@ to @

091020 change value of C386 from 10P to 22P

091029 add R376 0_0402_5% for EMI solution

0111Change BOM Structure of C390 from @ to mount
091020 change value of C390 from 10P to 22P

091015 add R801/R802 0ohm

0301 Change BOM Structure of R1289 and C388/C389/C393/C390 from NOR_CLK@ to @

091210 add C392/C393 22P for RF team

Add 1K follow Intel check list 05/11

Follow Intel check list change to 27P 06/05

Rename 06/06

Add CLK to GPU 09/10/08

Add PEG_CLKREQ# 09/10/08 PU to +3VS

Add WWAN_CLKREQ# 05/04

Add LAN_CLKREQ# 091116

0303 change U4 P/N from SA00003H730 to SA00003H610

For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#

For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

For PCI2_TME:0=Overclocking of CPU and SRC allowed
(ICS only) 1=Overclocking of CPU and SRC NOT allowed

Routing the trace at least 10mil

SRC PORT LIST

PORT	DEVICE
SRC1	CPU_SSCDREFCLK
SRC2	
SRC3	PCIE_VGA
SRC4	PCIE_WLAN
SRC6	PCIE_SATA
SRC7	PCIE_PCH
SRC8	CPU_ITP
SRC9	CLK_CPU_EXP
SRC10	PCIE_LAN
SRC11	PCIE_WWAN

REQ PORT LIST

PORT	DEVICE
REQ_3#	PCIE_VGA
REQ_4#	PCIE_WLAN
REQ_6#	
REQ_7#	
REQ_9#	
REQ_10#	PCIE_LAN
REQ_11#	PCIE_WWAN
REQ_A#	

SLG8SP556VTR_QFN72_10X10

Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

Compal Electronics, Inc.

Title: Clock Generator CK505

Size: | Document Number: NAVD0 LA-6091P | Rev: 1.0

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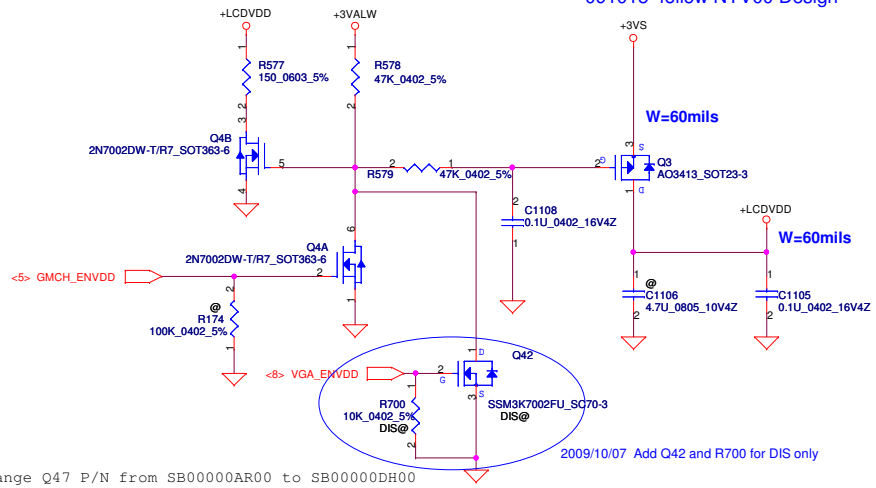
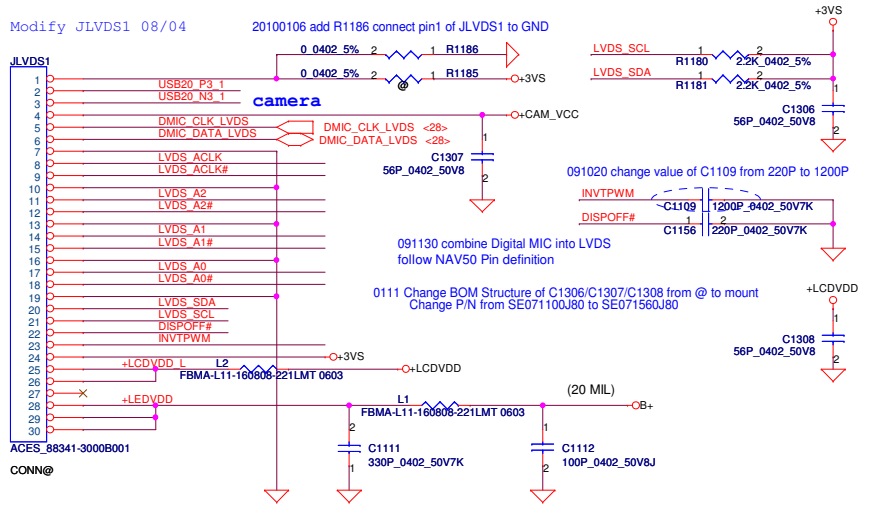
LCD POWER CIRCUIT

091015 follow NTV00 Design

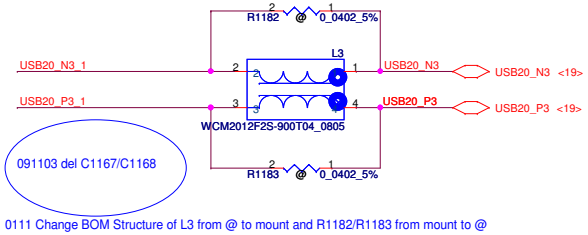


100112 change Q47 P/N from SB00000AR00 to SB00000DH00

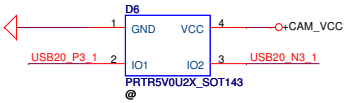
CMOS & LCD/PANEL BD. Conn.



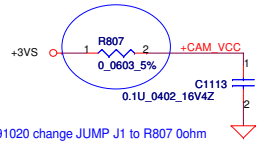
LED PANEL Conn.



0111 Change BOM Structure of L3 from @ to mount and R1182/R1183 from mount to @

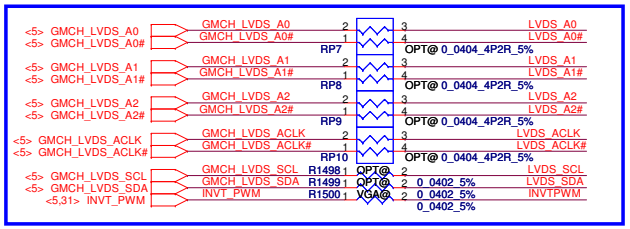


091203 change P/N of D6 to SC300000100



091020 change JUMP J1 to R807 0ohm

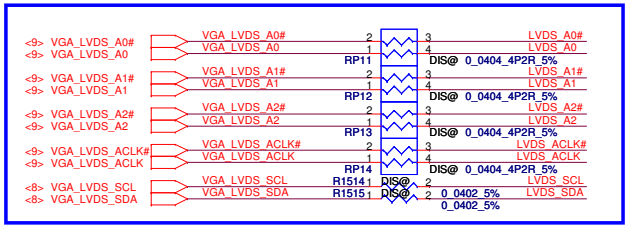
OPTIMUS



091202 swap A0/A0#,A1/A1#,A2/A2#,ACLK/ACLK#
nets on RP7/RP8/RP9/RP10

091209 change BOM Structure of R1500 from OPT@ to VGA@

DIS ONLY



091202 swap A0/A0#,A1/A1#,A2/A2#,ACLK/ACLK#
nets on RP11/RP12/RP13/RP14

Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

Compal Electronics, Inc.

Title: LVDS /INVERTER

Size	Document Number	Rev
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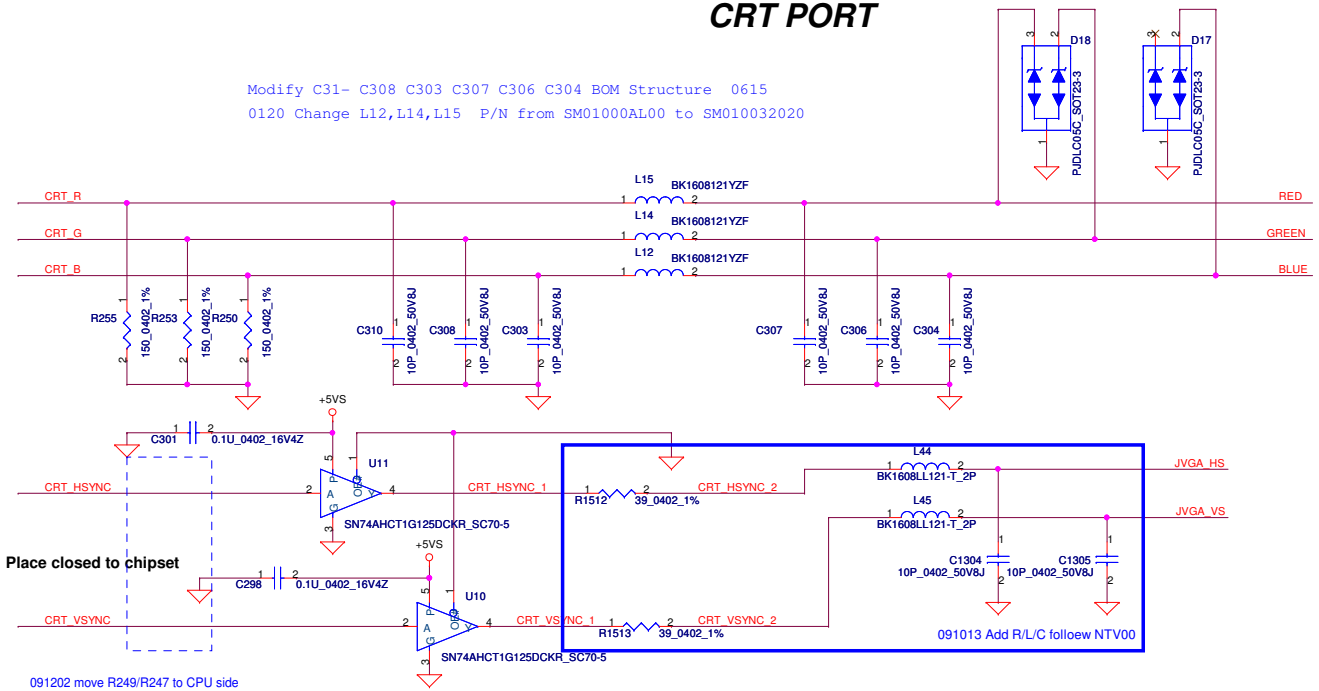
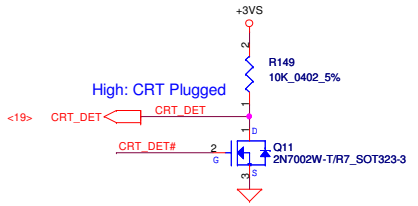
CRT PORT

Close to CRT CONN for ESD.

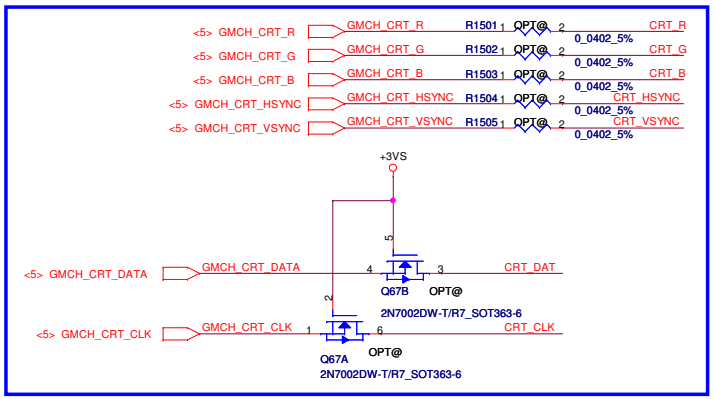
Modify C31- C308 C303 C307 C306 C304 BOM Structure 0615

0120 Change L12,L14,L15 P/N from SM01000AL00 to SM010032020

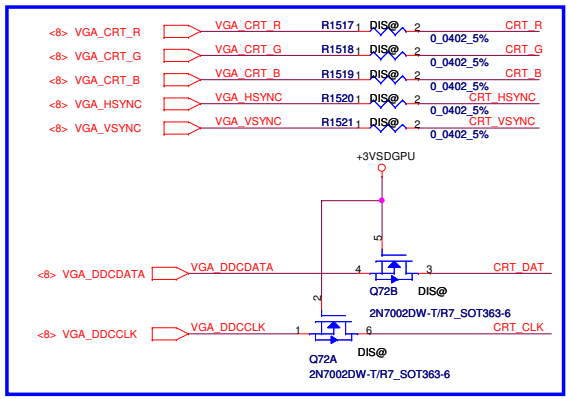




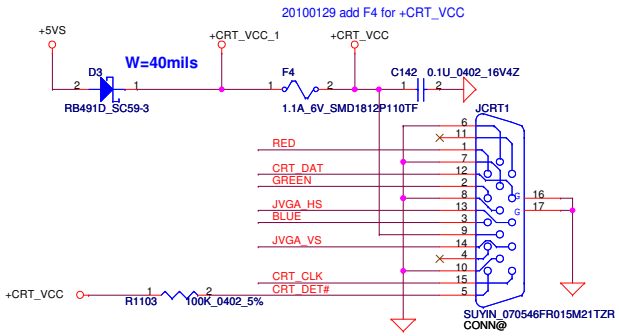
OPTIMUS

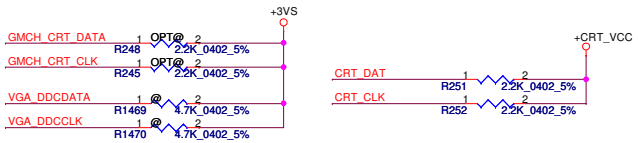


DIS ONLY



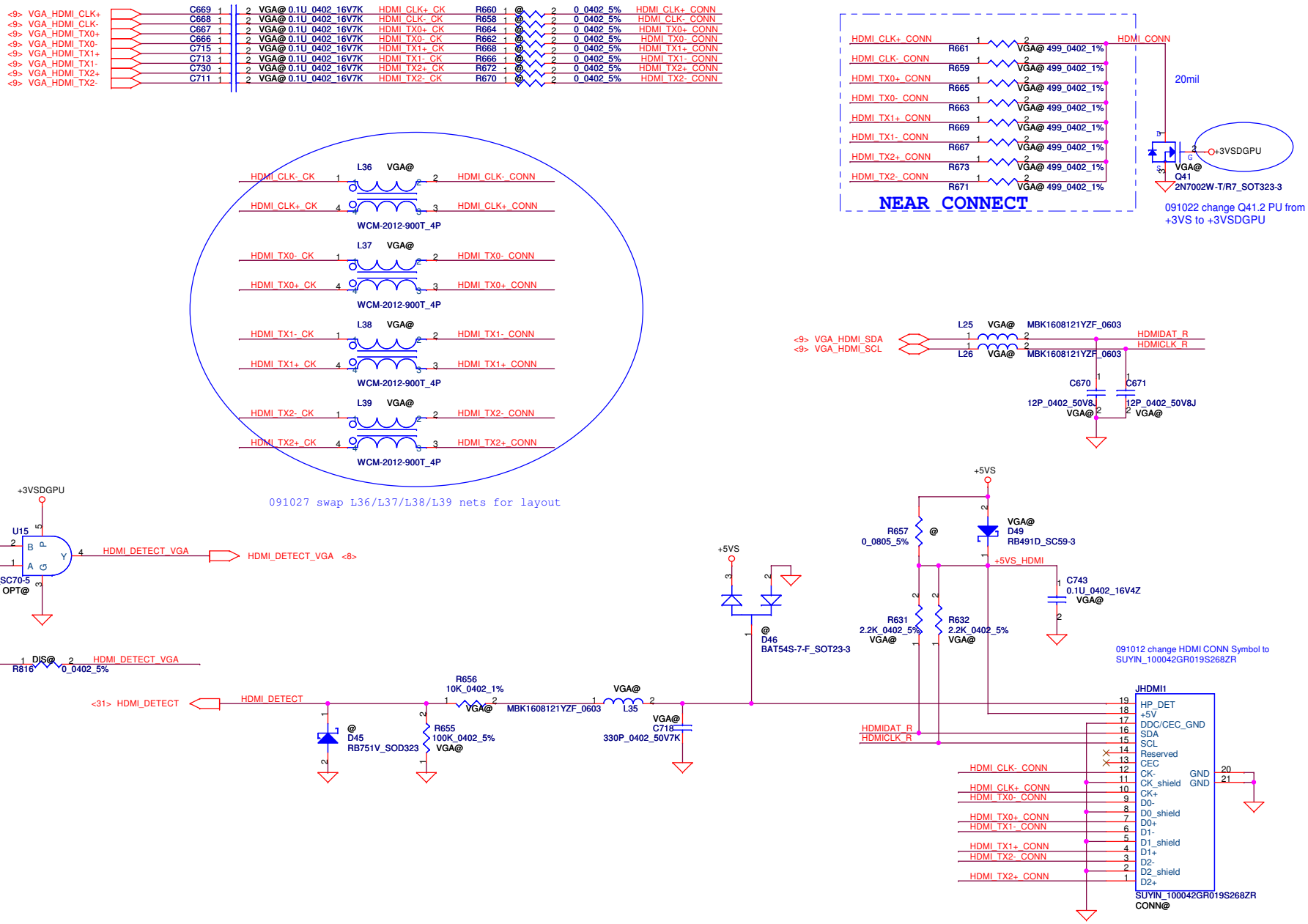
100112 change Q72 P/N from SB00000AR00 to SB00000DH00





Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

Compal Electronics, Inc.			
Title: CRT PORT			
Size: Custom	Document Number: NAVD0 LA-6091P		Rev: 1.0
Date: Wednesday, March 03, 2010		Sheet 15 of 46	



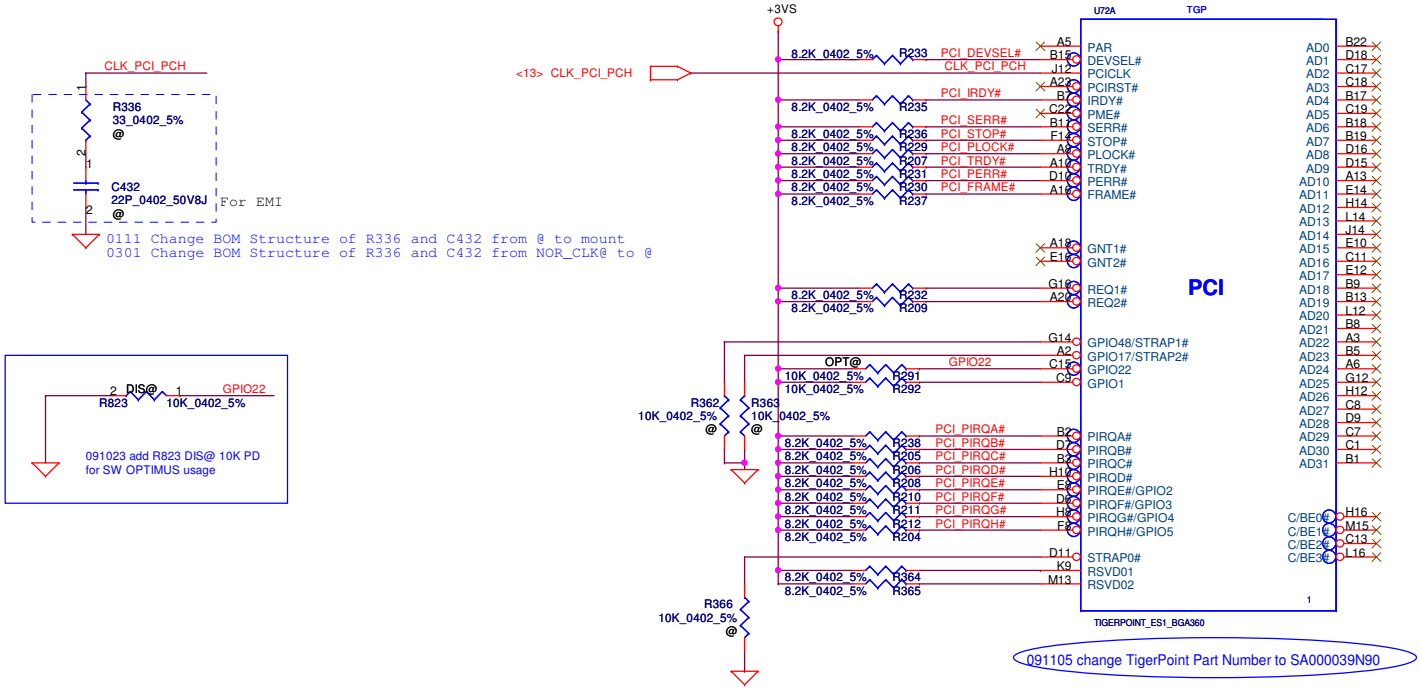
Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

Compal Electronics, Inc.

Title: HDMI CONN

Size	Document Number	Rev
Custom	NAVD0 LA-6091P	1.0

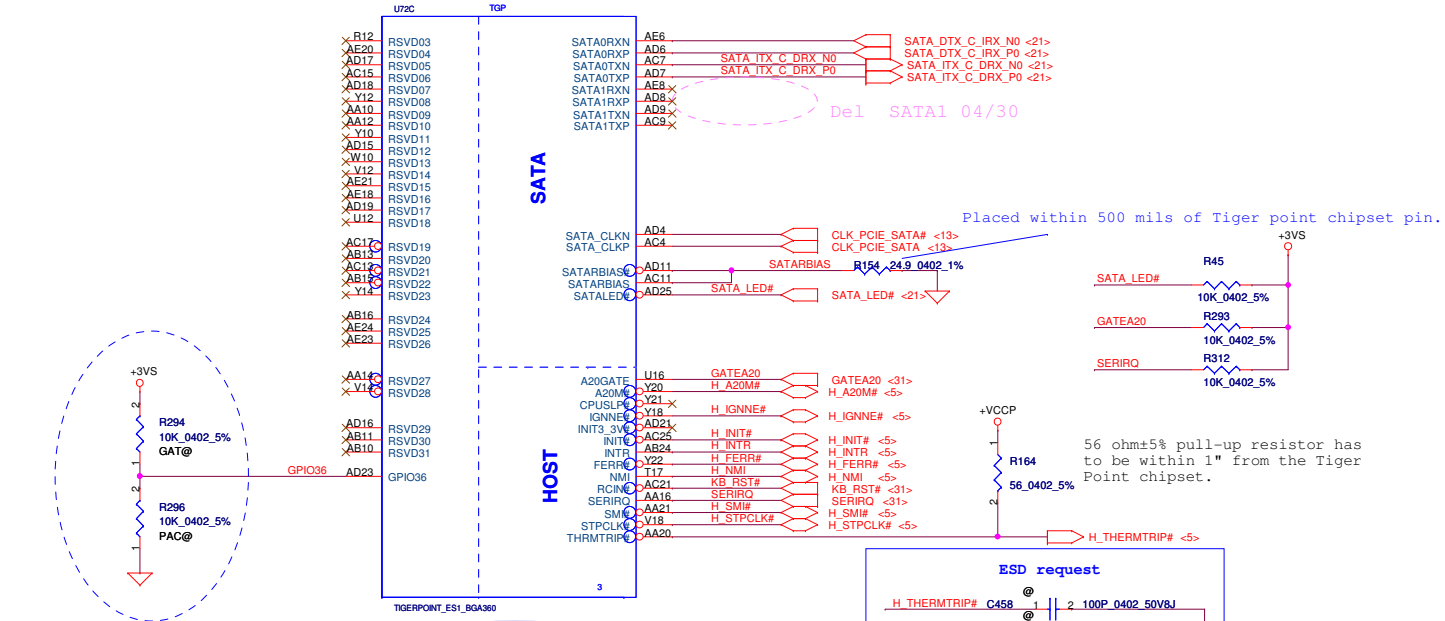
Date: Wednesday, March 03, 2010 Sheet 16 of 46



STRAP2# GPIO17	STRAP1# GPIO48	Boot BIOS
0	1	SPI
1	0	PCI
1	1	LPC

Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

Compal Electronics, Inc.	
Title	Tigerpoint(1/4)
Size	Document Number: NAVD0 LA-6091P
Rev	1.0
Date: Wednesday, March 03, 2010	Sheet 17 of 46



Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

Compal Electronics, Inc.			
Title: Tigerpoint(2/4)			
Size: Custom	Document Number: NAVD0 LA-6091P		Rev: 1.0
Date: Wednesday, March 03, 2010	Sheet 18 of 46		

PCIE	Port List
1	LAN
2	WLAN
3	WWAN
4	

USB	Port List
0	USB Left1
1	
2	USB Right2
3	CMOS
4	CardReader
5	WWAN
6	BT
7	WIMAX

091212 Add C30 near PCH
to prevent switch noise

HDA_SDIN0 C30 @100P_0402_50V8J

@ SW2 EVQPLHA15_4P RTCRST#

20100120 change SW2 from mount to @

ICH_SMBCLK C17 100P_0402_50V8J
ICH_SMBDATA C18 100P_0402_50V8J

091212 Add C17 C18 near U72
to prevent switch noise

091105 change TigerPoint Part Number to SA000039N90

U72D TGP

LPC: LAD0/FWH0, LAD1/FWH1, LAD2/FWH2, LAD3/FWH3, LDRQ0#, LFRAME#/FWH4
AUDIO: HDA_BIT_CLK, HDA_RST#, HDA_SDIN0, HDA_SDIN1, HDA_SDIN2, HDA_SDOUT, HDA_SYNC, CLK14
EPROM: EE_CS, EE_DIN, EE_DOUT, EE_SHCLK
LAN: LAN_CLK, LANR_RSTSYNC, LAN_RSTSYNC, LAN_RXD0, LAN_RXD1, LAN_RXD2, LAN_TXD0, LAN_TXD1, LAN_TXD2
RTC: RTCX1, RTCX2, RTCRST#
SMB: SMBALERT#/GPIO11, SMBCLK, SMBDATA, LINKALERT#, SMLINK0, SMLINK1
SPI: SPI_MISO, SPI_MOSI, SPI_CS#, SPI_CLK, SPI_ARB
MISC: BMBUSY#/GPIO0, GPIO6, GPIO7, GPIO8, GPIO9, GPIO10, GPIO12, GPIO13, GPIO14, GPIO15, DPRSLPVR, STP_PCI#, STP_CPU#, GPIO24, GPIO25, GPIO26, GPIO27, GPIO28, CLKRUN#, GPIO33, GPIO34, GPIO38, GPIO39, CPUPWRGD/GPIO49, THRM#, VRMPWRGD, MCH_SYNC#, PWRBTN#, RI#, SUS_STAT#/LPCPD#, SUSCLK, SYS_RESET#, PLTRST#, WAKE#, INTRUDER#, PWROK, RSMRST#, INTVRMEN, SPKR, SLP_S3#, SLP_S4#, SLP_S5#, BATLOW#, DPRSTP#, DPSLP#, RSVD31

<31> LPC_AD0
<31> LPC_AD1
<31> LPC_AD2
<31> LPC_AD3
<31> LPC_FRAME#
<28,30> HDA_BITCLK_AUDIO
<28,30> HDA_RST_AUDIO#
<28> HDA_SDIN0
<28,30> HDA_SDOUT_AUDIO
<28,30> HDA_SYNC_AUDIO
<13> CLK_PCH_14M

R337 33_0402_5%
C433 22P_0402_50V8J
For EMI, Close to TigerPoint

<13> ICH_SMBCLK
<13> ICH_SMBDATA

Change EC_LID_OUT# From GPIO13 to GPIO11
06/08

GPIO0 CRT_DET CRT_DET <15>
GPIO7 EC_SMI# EC_SMI# <31>
GPIO8 EC_SCI# EC_SCI# <31>
GPIO12 EC_LID_OUT# EC_LID_OUT# <31>
GPIO14 GPIO15 PM_DPRSLPVR <5>
H_STP_PCI# <13>
H_STP_CPU# <13>
1K_0402_5%
PM_CLKRUN#
GPIO38
GPIO39
H_PWRGD H_PWRGD <5>
EC_THERM# EC_THERM# <31>
VGATE
MCH_SYNC#
PBTN_OUT# PBTN_OUT# <31>
ICH_RI#
SYS_RST#
PLTRST# <5,8,24,25,26,31>
ICH_PCIE_WAKE# <24,25>
INTRUDER#
T_PWROK
EC_RSMRST#R
INTVRMEN
SB_SPKR SB_SPKR <29>
PM_SLP_S3# <31>
PM_SLP_S4# <31>
PM_SLP_S5# <31>
PM_BATT_LOW#
H_DPRSTP# <5>
H_DPSLP# <5>

091105 change TigerPoint Part Number to SA000039N90

091204 add USB20_N1/P1 for
SIM CARD Conn.

U72B TGP

DMI: DMI0RXN, DMI0RXP, DMI0TXN, DMI0TXP, DMI1RXN, DMI1RXP, DMI1TXN, DMI1TXP, DMI2RXN, DMI2RXP, DMI2TXN, DMI2TXP, DMI3RXN, DMI3RXP, DMI3TXN, DMI3TXP
PCIE: PERN1, PERP1, PETN1, PETP1, PERN2, PERP2, PETN2, PETP2, PERN3, PERP3, PETN3, PETP3, PERN4, PERP4, PETN4, PETP4, DMI_ZCOMP, DMI_IRCOMP, DMI_CLKN, DMI_CLKP
USB: USBP0N, USBP0P, USBP1N, USBP1P, USBP2N, USBP2P, USBP3N, USBP3P, USBP4N, USBP4P, USBP5N, USBP5P, USBP6N, USBP6P, USBP7N, USBP7P, OC0#, OC1#, OC2#, OC3#, OC4#, OC5#/GPIO29, OC6#/GPIO30, OC7#/GPIO31, USBRBIAS, USBRBIAS#, CLK48

<4> DMI_TX#0
<4> DMI_TX0
<4> DMI_RX#0
<4> DMI_RX0
<4> DMI_TX#1
<4> DMI_TX1
<4> DMI_RX#1
<4> DMI_RX1

<26> PCIE_DTX_C_IRX_N1
<26> PCIE_DTX_C_IRX_P1
<26> PCIE_ITX_C_DRX_N1
<26> PCIE_ITX_C_DRX_P1
<25> PCIE_DTX_C_IRX_N2
<25> PCIE_DTX_C_IRX_P2
<25> PCIE_ITX_C_DRX_N2
<25> PCIE_ITX_C_DRX_P2
<24> PCIE_DTX_C_IRX_N3
<24> PCIE_DTX_C_IRX_P3
<24> PCIE_ITX_C_DRX_N3
<24> PCIE_ITX_C_DRX_P3
<8> PCIE_CRX_GTX_N0
<8> PCIE_CRX_GTX_P0
<8> PCIE_CTX_GRX_N0
<8> PCIE_CTX_GRX_P0

C565 0.1U_0402_10V7K PCIE_ITX_C_DRX_N1
C566 0.1U_0402_10V7K PCIE_ITX_C_DRX_P1
C53 0.1U_0402_10V7K PCIE_ITX_C_DRX_N2
C49 0.1U_0402_10V7K PCIE_ITX_C_DRX_P2
C52 0.1U_0402_10V7K PCIE_ITX_C_DRX_N3
C54 0.1U_0402_10V7K PCIE_ITX_C_DRX_P3
VGA@
C1277 0.1U_0402_10V7K PCIE_CTX_C_GRX_N0
C1278 0.1U_0402_10V7K PCIE_CTX_C_GRX_P0
VGA@

09/10/08 Add PCIE to GPU

USB_OC#0 C50 @100P_0402_50V8J
091212 Add C50 near PCH
to prevent switch noise

+1.5VS
R153 24.9_0402_1%
DMI_COMP

<13> CLK_PCIE_PCH#
<13> CLK_PCIE_PCH

USB20_N0 USB20_N0 <23>
USB20_P0 USB20_P0 <23>
USB20_N1_R R225 0_0402_5% USB20_N1 USB20_N1 <24>
USB20_P1_R R226 0_0402_5% USB20_P1 USB20_P1 <24>
USB20_N1_R USB20_N1 <23>
USB20_P1_R USB20_P1 <23>
USB20_N2 USB20_N2 <23>
USB20_P2 USB20_P2 <23>
USB20_N3 USB20_N3 <14>
USB20_P3 USB20_P3 <14>
USB20_N4 USB20_N4 <27>
USB20_P4 USB20_P4 <27>
USB20_N5 USB20_N5 <24>
USB20_P5 USB20_P5 <24>
USB20_N6 USB20_N6 <24>
USB20_P6 USB20_P6 <24>
USB20_N7 USB20_N7 <25>
USB20_P7 USB20_P7 <25>

USB_OC#0 USB_OC#0 <23>
USB_OC#3_7 USB_OC#3_7
USB_OC#2 USB_OC#2 <23>

USBRBIAS R152 22.6_0402_1%

CLK_PCH_48M CLK_PCH_48M <13>
R338 33_0402_5% @
C434 22P_0402_50V8J @
For EMI, Close to TigerPoint

091113 change net name from
USB_OC#0_1 to USB_OC#0
add net name USB_OC#1
USB_OC#0 R47 10K_0402_5%
USB_OC#2 R49 10K_0402_5%
USB_OC#3_7 R48 10K_0402_5%
091020 change net name from
USB_OC#3/4/5/6/7 to USB_OC#3_7

TIGERPOINT_ES1_BGA360

+3VALW
2.2K_0402_5% R147 ICH_SMBCLK
2.2K_0402_5% R148 ICH_SMBDATA
10K_0402_5% R40 LINKALERT#
10K_0402_5% R44 SMLINK0
10K_0402_5% R43 SMLINK1
8.2K_0402_5% R239 PM_BATT_LOW#
1K_0402_5% R145 ICH_PCIE_WAKE#
10K_0402_5% R39 SYS_RST#
8.2K_0402_5% R240 ICH_RI#
10K_0402_5% R36 EC_LID_OUT#
8.2K_0402_5% R314 GPIO12
8.2K_0402_5% R315 GPIO14
8.2K_0402_5% R316 GPIO15
8.2K_0402_5% R301 SMBALERT#

+RTCVCC
1M_0402_5% R146 INTRUDER#
R197 INTVRMEN
332K_0402_1%

+RTCVCC R196 20K_0402_5% RTCRST#
R1184 @ 0_0402_5%
C230 1U_0603_10V4Z~D
J14 @ JUMP_43X39
Change J3 to R1184 4/29
20100129 Add J14 for RTCRST#

10K_0402_5% R37 T_PWROK
10K_0402_5% R38 EC_RSMRST#R

+3VS
10K_0402_5% R42 MCH_SYNC#
8.2K_0402_5% R295 GPIO7
8.2K_0402_5% R308 EC_THERM#
8.2K_0402_5% R302 GPIO0
8.2K_0402_5% R241 PM_CLKRUN#

091020 add R806 22ohm for 3G noise solution
0111 Change BOM Structure of R806 and C1214 from @ to mount
0111 Change R806 value from 22_0402_5% ohm to 0_0402_5%
2003 delete R806 for RF

HDA_BITCLK_AUDIO C1214 22P_0402_50V8J
Del R203 (pull-up GPIO6 Resister) 06/08
0120 Change C368,C371 from 15p to 12p

C368 12P_0402_50V8J RTCX1
Routing the trace at least 10mil
Y3 NC OSC NC OSC 32.768KHZ_12.5PF_Q13MC14610002
R288 10M_0402_5%
C371 12P_0402_50V8J RTCX2

+3VS
R1376 10K_0402_5% D0@
GPIO38
R1377 10K_0402_5% E0@
R1380 8.2K_0402_5% NON3G_LCD@
GPIO39
R1379 8.2K_0402_5% 3G_LG@
0112 Add R1379,R1380 10K_0402_5% for GPIO39

ACIN_C
+3VALW
R223 100K_0402_5%
D25 RB751V_SOD323 ACIN
R222 @ 0_0402_5%
ACIN <31,38>

0118 Change C1158 from 220p to 100K ohm
0131 Change C1158 symbol

PLTRST#
R1598 100K_0402_5%
For ESD

+RTCVCC
R1370 1K_0402_5% +RTCBATT
D37 BAS40-04_SOT23-3
C1148 0.1U_0402_16V4Z
+CHGRTC
Add +RTCVCC circuit 06/12

RSMRST circuit
R372 0_0402_5%
<31> EC_RSMRST#
Q30 @MMBT3906_SOT23-3
EC_RSMRST#R
BAV99DW-7_SOT363
R373 @4.7K_0402_5% +3VALW
R374 @2.2K_0402_5%
D28B @ D28A BAV99DW-7_SOT363
R375 @2.2K_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

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Compal Electronics, Inc.
Title: Tigerpoint(3/4)
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091105 change TigerPoint Part Number to SA000039N90

TGP

U72E

POWER

VCC5REF	F12	+V5REF_RUN	6mA
VCC5REF_SUS	F5	+V5REF_SUS	10mA
VCCSATAPLL	Y6	+SATAPLL	50mA
VCCRTC	AE3	+RTCVCC	
VCCDMIPLL	Y25	+DMIPLL	
VCCUSBPLL	F6	10mA	
V_CPU_IO	W18	14mA	
VCC1_5_1 VCC1_5_2 VCC1_5_3 VCC1_5_4	AA8 M9 M20 N22	1.3A	+1.5VS
VCC1_05_1 VCC1_05_2 VCC1_05_3 VCC1_05_4	J10 K17 P15 V10	0.98A	+VCCP
VCC3_3_1 VCC3_3_2 VCC3_3_3 VCC3_3_4 VCC3_3_5 VCC3_3_6	H25 AD13 F10 G10 R10 T9	0.29A	+3VS
VCCSUS3_3_1 VCCSUS3_3_2 VCCSUS3_3_3 VCCSUS3_3_4	F18 N4 K7 F1	0.13A	+3VALW

TIGERPOINT_ES1_BGA360

+5VS +3VS R33 100_0402_5% D12 RB751V-40_SOD323-2 +V5REF_RUN C59 1U_0402_6.3V6K

+5VALW +3VALW R35 10_0402_5% D10 RB751V-40_SOD323-2 +V5REF_SUS C40 0.1U_0402_16V4Z

+VCCP C41 0.1U_0402_16V4Z

C42 0.1U_0402_16V4Z C47 0.01U_0402_16V7K

C48 0.1U_0402_16V4Z C45 0.1U_0402_16V4Z C61 1U_0402_6.3V6K C62 1U_0402_6.3V6K C459 10U_0603_6.3V6M

C46 0.1U_0402_16V4Z C60 1U_0402_6.3V6K C63 1U_0402_6.3V6K C460 10U_0603_6.3V6M

C43 0.1U_0402_16V4Z C37 0.1U_0402_16V4Z C38 1U_0402_6.3V6K C461 1U_0402_6.3V6K C462 1U_0402_6.3V6K

C39 0.1U_0402_16V4Z C44 1U_0402_6.3V6K C463 1U_0402_6.3V6K

Place closely pin Y25 within 100mlis.

+1.5VS R30 0_0603_5% 0.01U_0402_16V7K +DMIPLL C58 10U_0603_6.3V6M C28 C464 4.7U_0603_6.3V6K

Place closely pin Y6 within 100mlis.

+1.5VS R29 0_0603_5% +SATAPLL C57 10U_0603_6.3V6M C27 0.1U_0402_16V4Z

091105 change TigerPoint Part Number to SA000039N90

U72F TGP

VSS01	A1
VSS02	A25
VSS03	B6
VSS04	B10
VSS05	B16
VSS06	B20
VSS07	B24
VSS08	E18
VSS09	F16
VSS10	G4
VSS11	G8
VSS12	H1
VSS13	H4
VSS14	H5
VSS15	K4
VSS16	K8
VSS17	K11
VSS18	K19
VSS19	K20
VSS20	L4
VSS21	M7
VSS22	M11
VSS23	N3
VSS24	N12
VSS25	N13
VSS26	N14
VSS27	N23
VSS28	P11
VSS29	P13
VSS30	P19
VSS31	R14
VSS32	R22
VSS33	T2
VSS34	T22
VSS35	V1
VSS36	V7
VSS37	V8
VSS38	V19
VSS39	V22
VSS40	V25
VSS41	W12
VSS42	W22
VSS43	Y2
VSS44	Y24
VSS45	AB4
VSS46	AB6
VSS47	AB7
VSS48	AB8
VSS49	AC8
VSS50	AD2
VSS51	AD10
VSS52	AD20
VSS53	AD24
VSS54	AE1
VSS55	AE10
VSS56	AE25
VSS57	G24
VSS58	AE13
VSS59	F2
RSVD32	AE16

TIGERPOINT_ES1_BGA360

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Compal Electronics, Inc.

Title: Tigerpoint(4/4)

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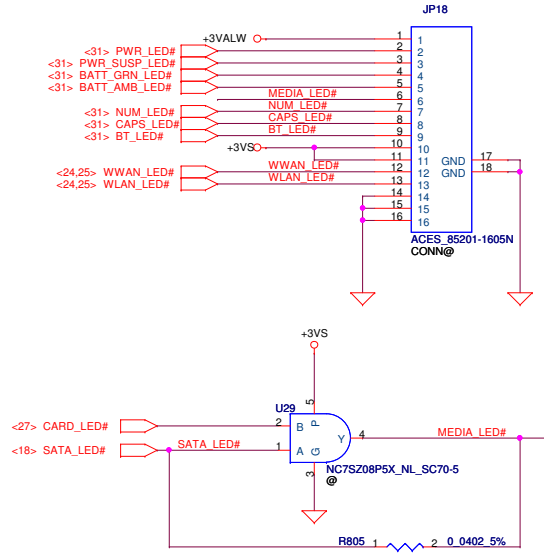
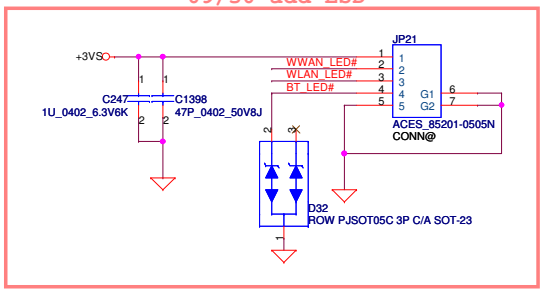
LED PCB CONN

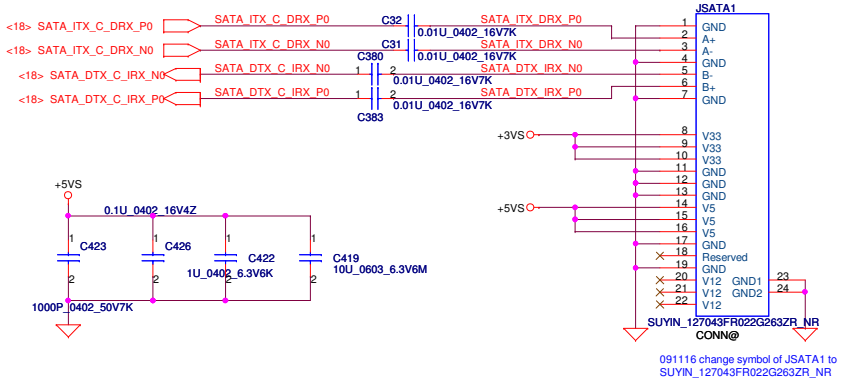


09/30 add ESD



0108 Add C247,C1398 on pin1 of JP21 (RF)

SATA HDD Conn.



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Compal Electronics, Inc.

Title: LED/HDD/Funotion Board CONN.

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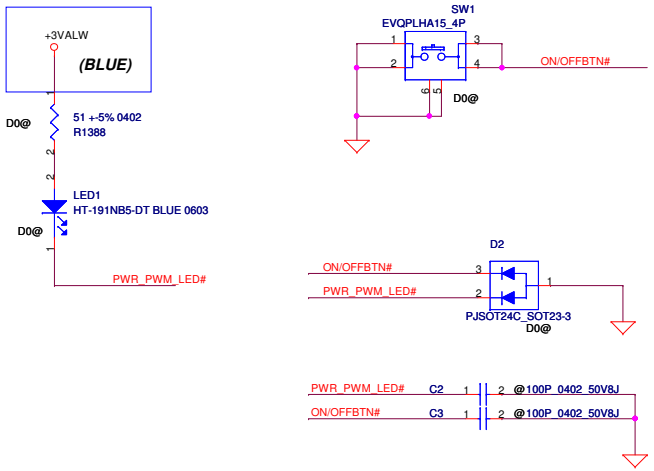
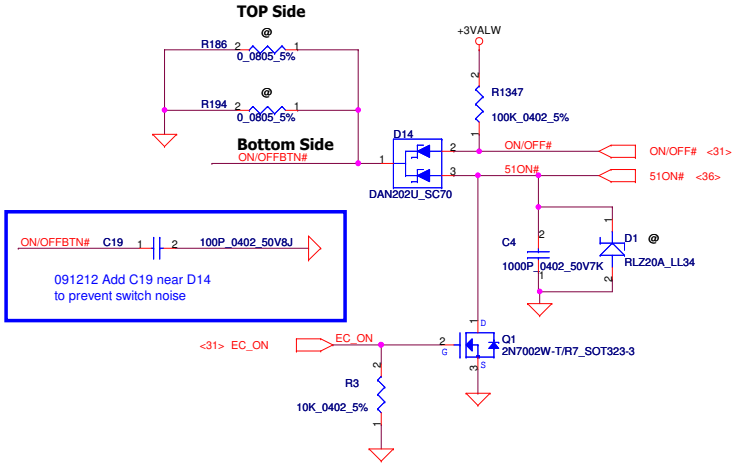
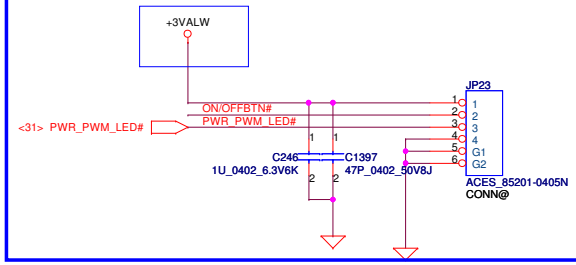
SW1





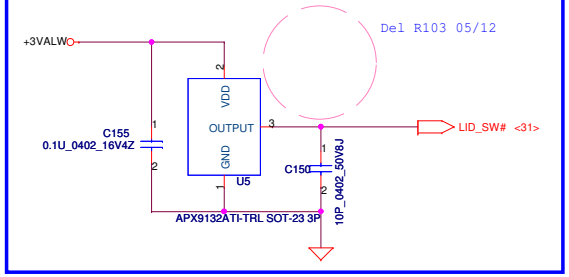
PWR/B Conn

091019 Change +3VS to +3VALW



0108 Add C246,C1397 on pin1 of JP23

LID Switch



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Compal Electronics, Inc.

Title: ON/OFF / PWR/B CONN./ LID SW

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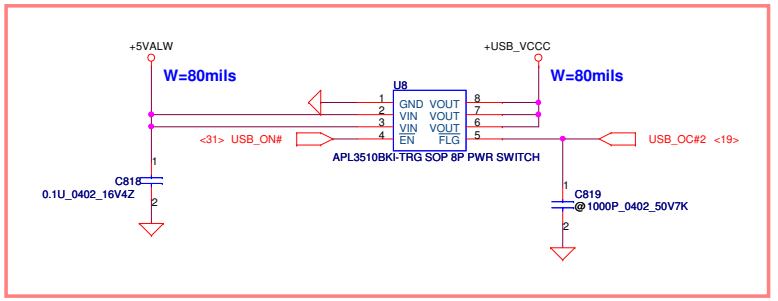
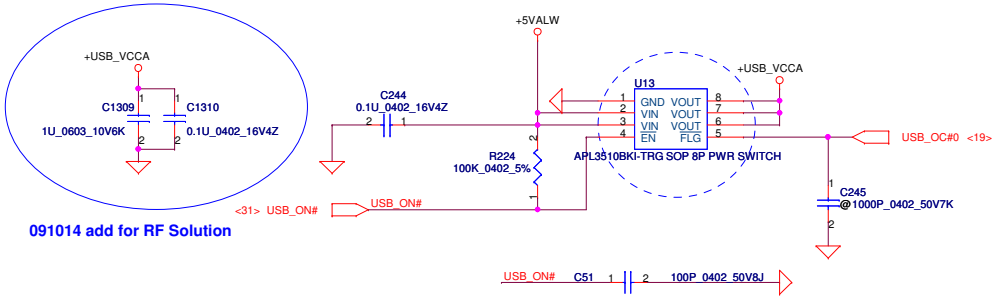
5/5 Add U2 circuit

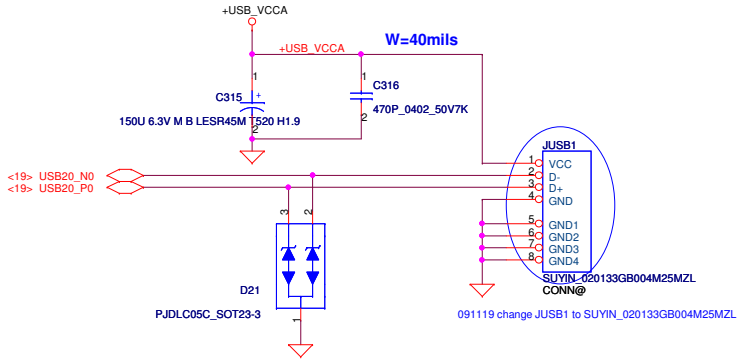




091014 add for RF Solution

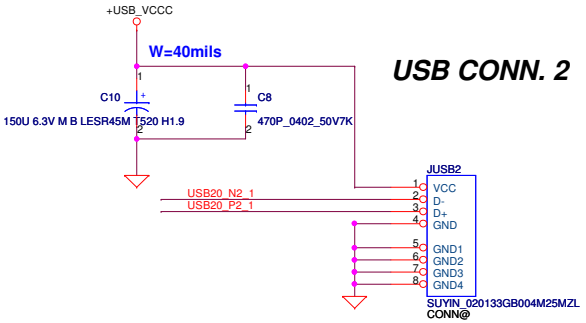
091212 Add C51 near U13
to prevent switch noise

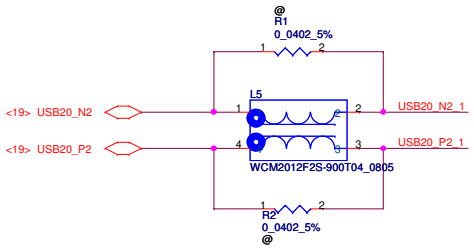
USB CONN.1



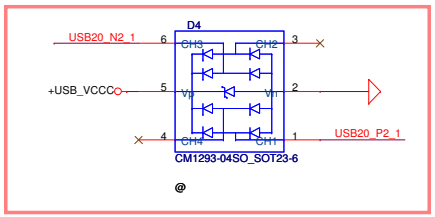
091119 change JUSB1 to SUYIN_020133GB004M25MZL

USB CONN. 2





5/12 Revised net name



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Title	USB PORT		
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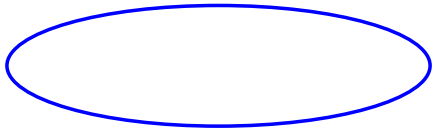
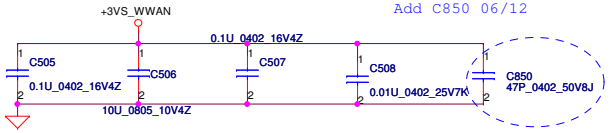
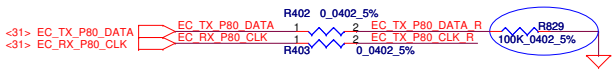
Mini-Express Card for WWAN

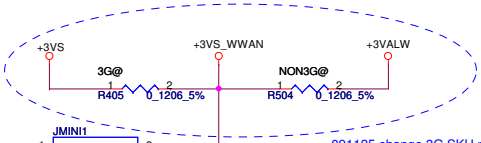
091019 Remove C1163/C1164/C1165/C1166



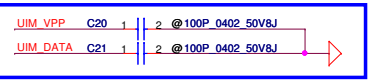


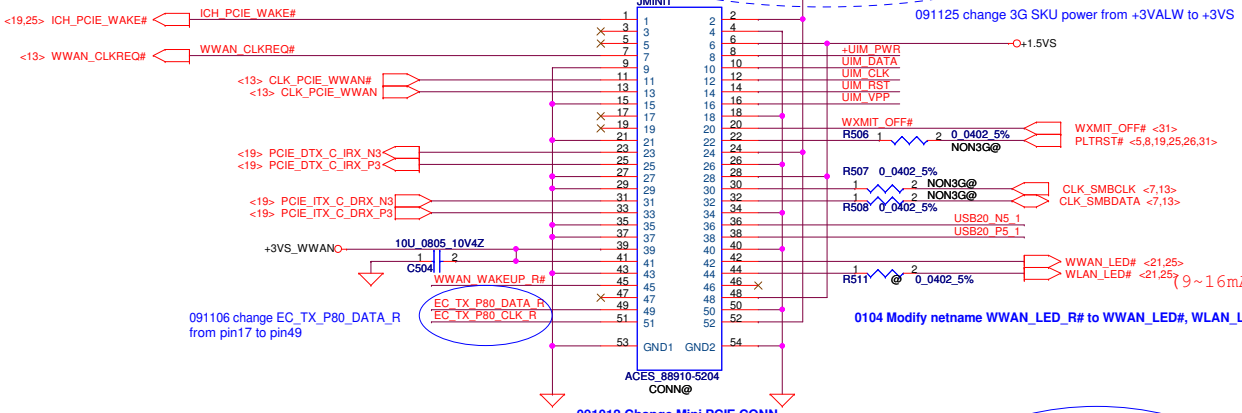
091106 add R829 100K PD to GND





091212 Add C20, C21 near JMINI1 to prevent switch noise





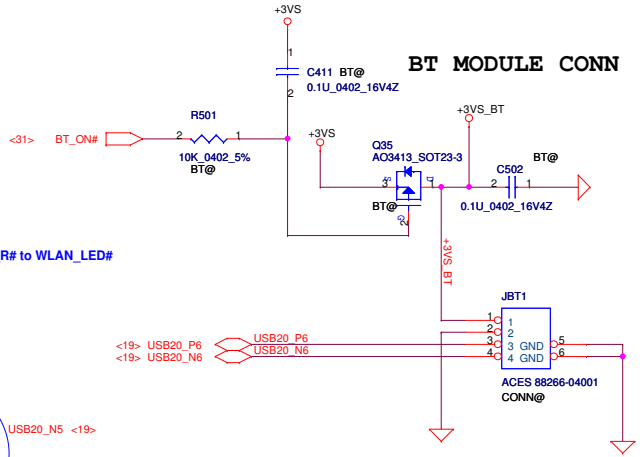
091106 change EC_TX_P80_DATA_R from pin17 to pin49

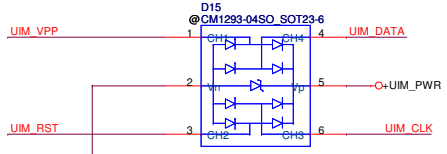
091125 change 3G SKU power from +3VALW to +3VS

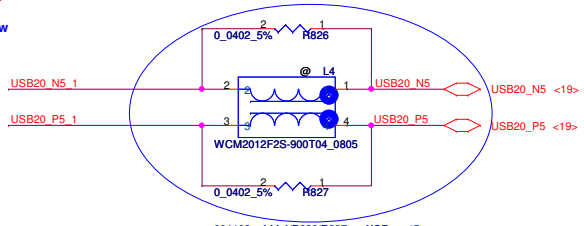
0104 Modify netname WWAN_LED_R# to WWAN_LED#, WLAN_LED_R# to WLAN_LED#

091012 Change Mini PCIE CONN Symbol to ACES 88910-5204 follow ME CONN LISTRev08

BT MODULE CONN

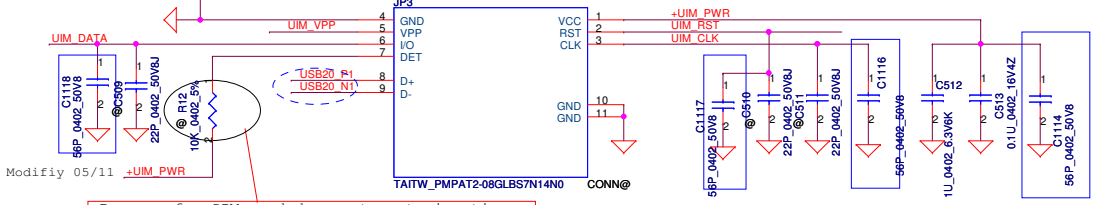






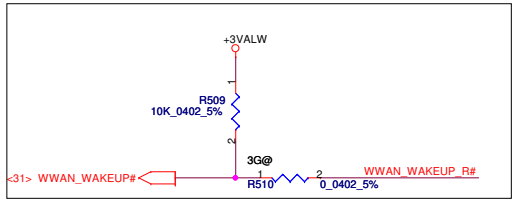
091102 add L4/R826/R827 on USB port5 follow RF team review

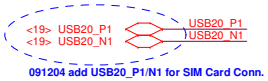
091204 change SIM Card Conn. to TAITW_PMPAT2-08GLBS7N14N0



Reserve for SIM card does not meet rise time and pull-up is needed.

Add C1114 C1116 C1117 C1118 05/11
Change C512 to 1U_0402 05/14





091204 add USB20_P1/N1 for SIM Card Conn.

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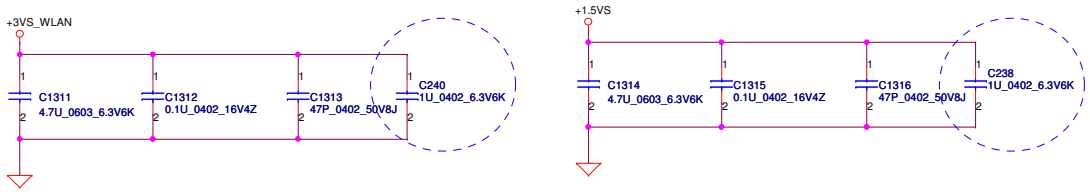
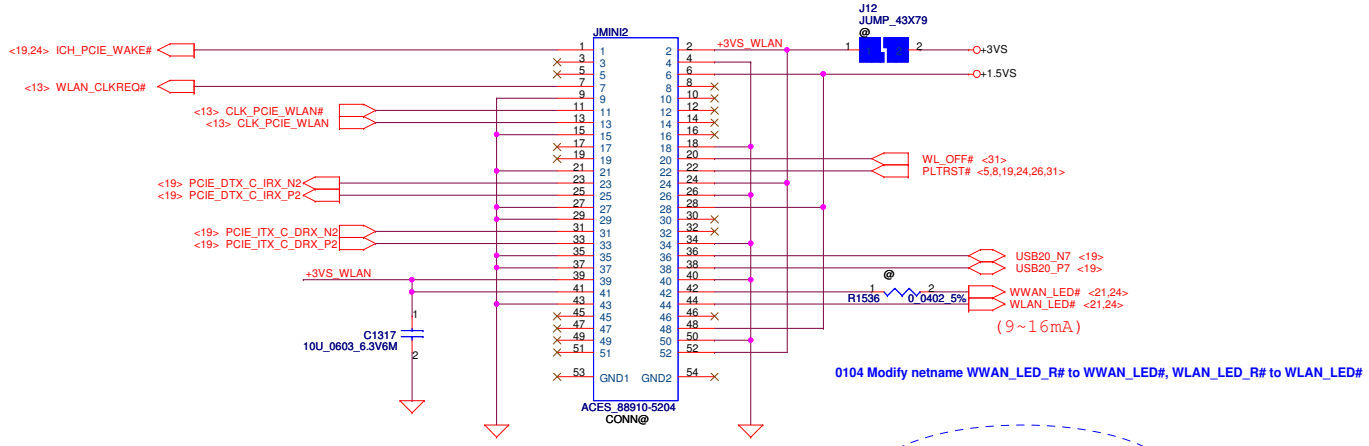
Mini-Express Card for WLAN



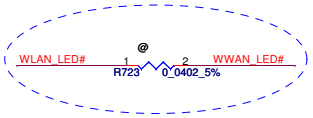
091127 reserve C240/C238 for RF team

0111 Change BOM Structure of C238/C240 from @ to mount



0104 Modify netname WWAN_LED_R# to WWAN_LED#, WLAN_LED_R# to WLAN_LED#

091116 Change JMINI2
Symbol to ACES 88910-5204 follow
ME CONN LIST 1116 Rev01



091125 reserve 0ohm for WIMAX

5/12 Update WLAN connector(the same as KAV60)
6/1 Revised 37、39、41、42、43 to NC
6/12 Update connector to DC040006S00
6/26 Update JMINI1 footprint
7/01 update pin 23,25,31,33

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Compal Electronics, Inc.

Title: WLAN

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C1319 close to pin6
C1318 close to pin2
C1320 close to pin5
60mil
40mil
1013 pull up R1537 (Vendor)
1013 Add R1538,R1539 for reserve 0.1u cap (Vendor)
U88
Atheros
AR8132 10/100 LAN
AR8132-AL1E_QFN48_6X6
C1324、C1325 close to U1
R1541 keep away other singal (25mil)
20mil
091116 change P/N of Y7 to SJ100003300
C1321,C1322,C1323 close to pin2 (<400mil)
C1326 close to pin11
close to pin42
30mil
L46 close to pin1 (<200mil)
C1330、C1331 close to L1 (<200mil)
the GND directly connect to GND layer
Place Close to Chip
20mil
the GND directly connect to GND layer
close to JRJ1
RJ45 CONN
JRJ1
SANTA_130452-3
CONN@
40mil
1013 Add C1348,C1349 for ESD (Vendor)
C1334,C1335 close to pin8
1013 Add C22 close to pin39 (Vendor)
C1336 close to pin16
C1337,C1338 close to pin22 .36
C1343 close to pin28
C1344 close to pin32
C1345 close to pin45
C1342 close to pin46
C1350 close to pin15
C1351 close to pin19
C1352 close to pin25
1013 Add R1550,C1353 for EMI (Vendor)
T80
350uH_NS0013LF

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Compal Electronics, Inc.

Title: LAN AR8132

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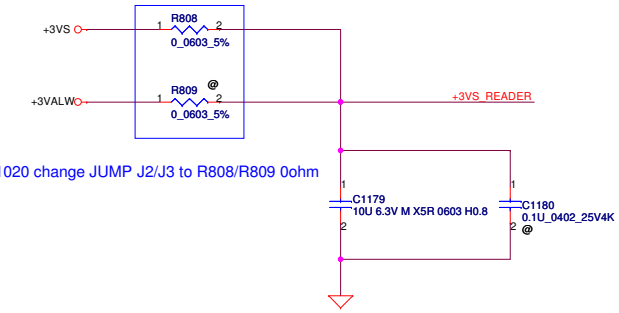
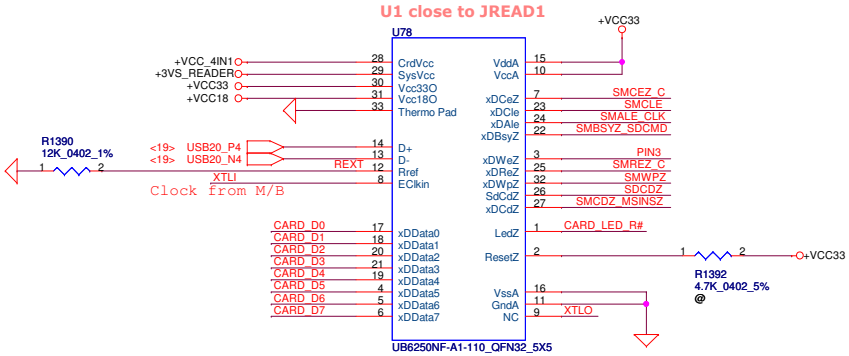
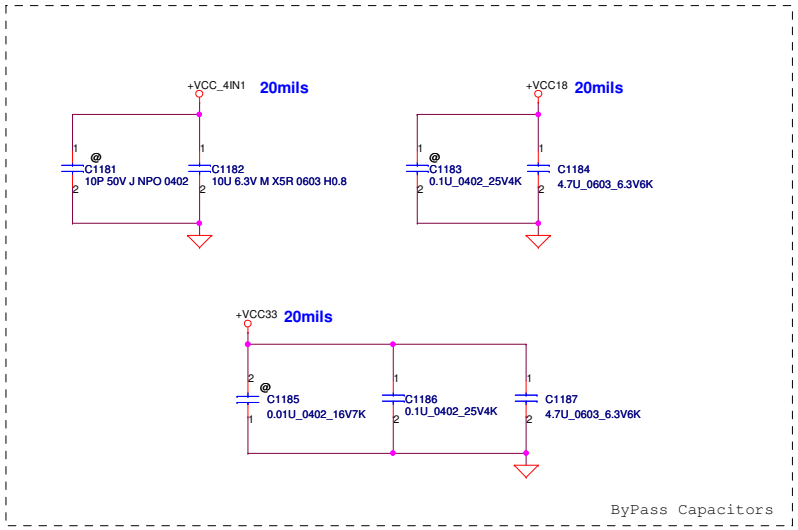
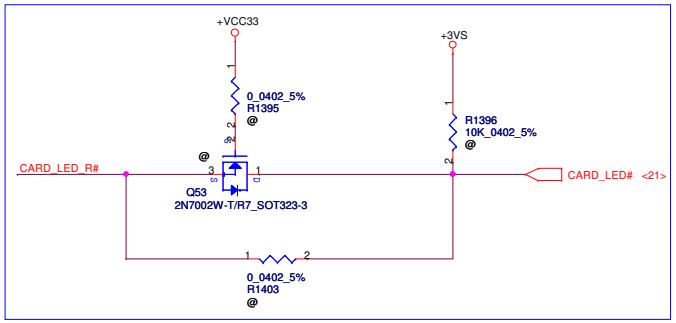




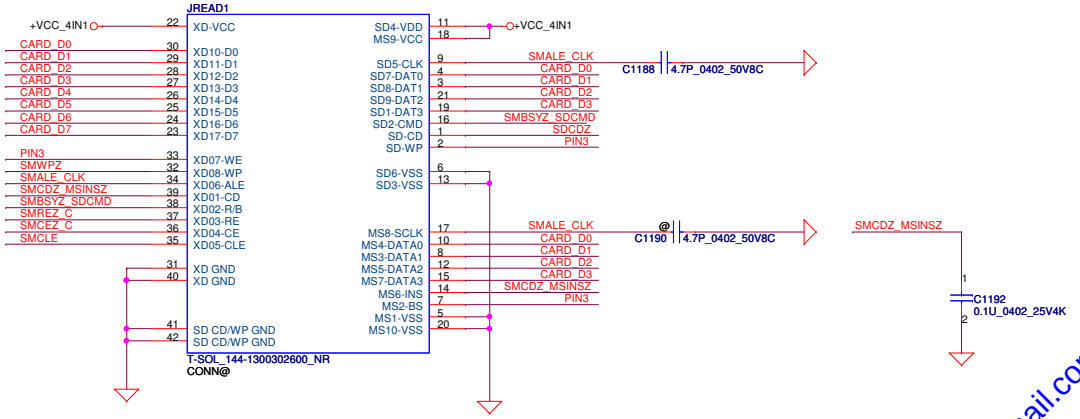
If use external crystal(Y6),
U78 will change UB6252

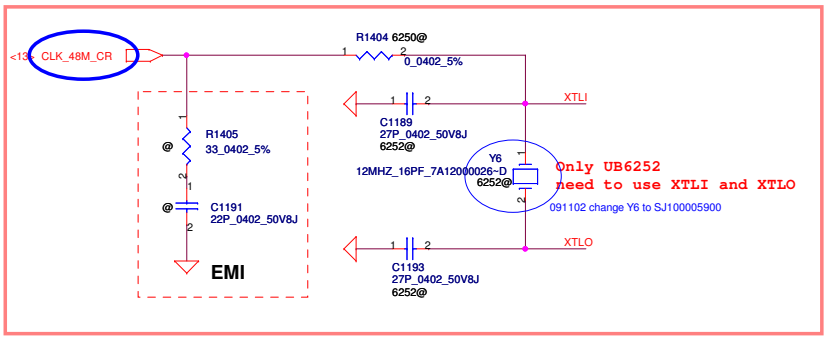




091203 change BOM structure of
Q53/R1395/R1396 from mount to @

Card Reader Connector





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Compal Electronics, Inc.

Title: CARD READER

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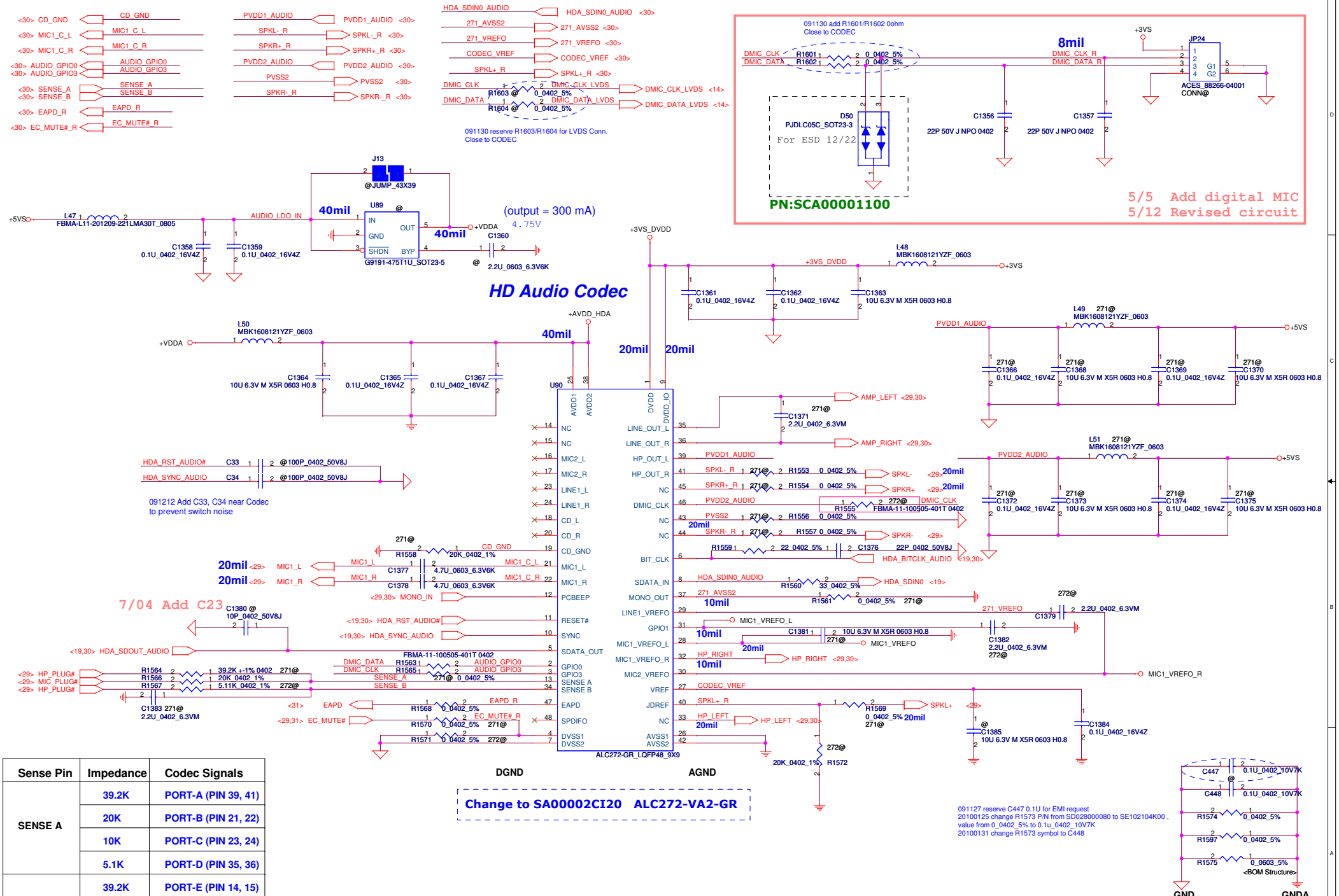


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

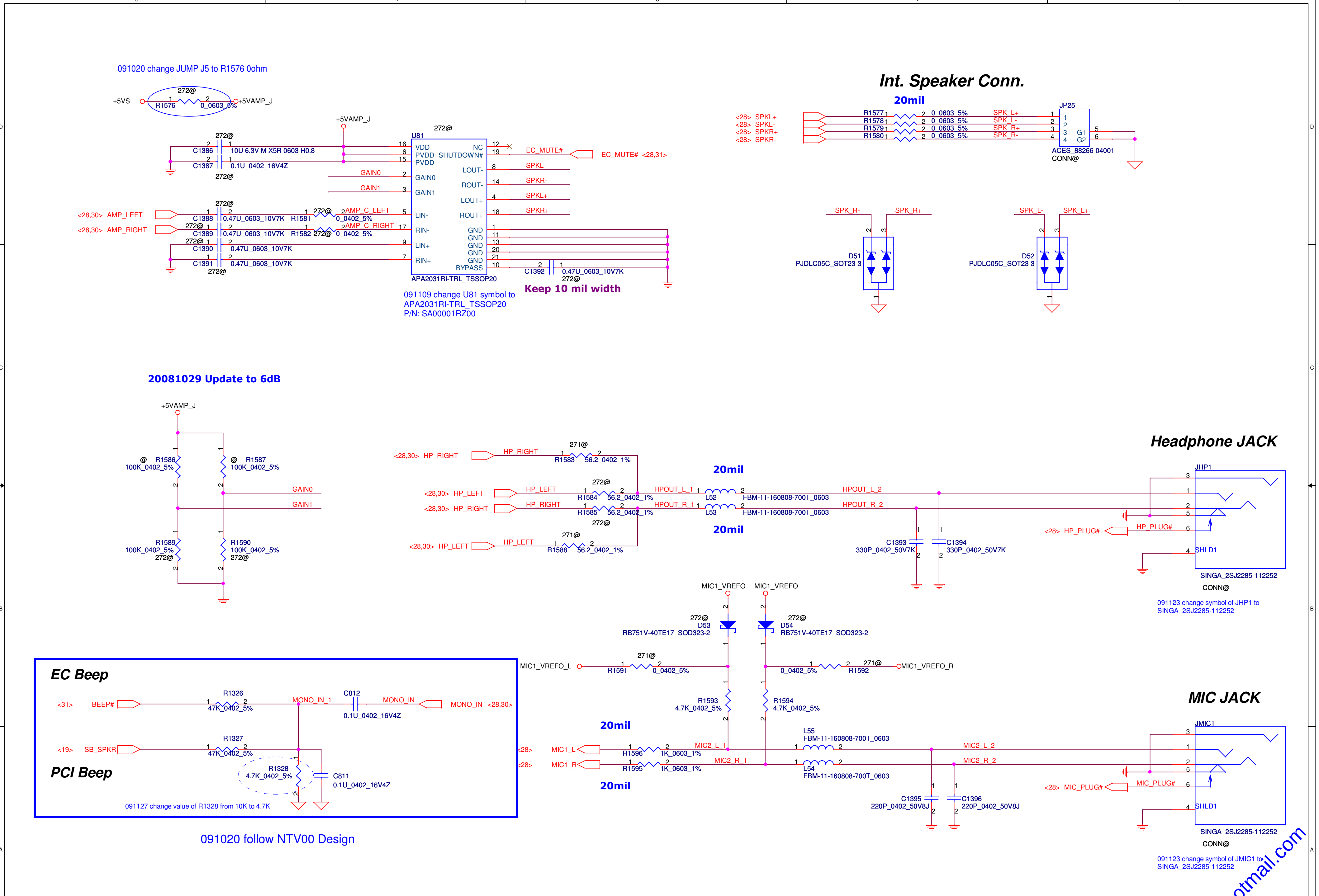
Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

Compal Electronics, Inc.

Title: AUDIO CODEC ALC272

Size: Custom | Document Number: NAVD0 LA-6091P | Rev: 1.0

Date: Wednesday, March 03, 2010 | Sheet 28 of 46



091020 change JUMP J5 to R1576 0ohm
+5VS
R1576
0_0603_5%
+5VAMP_J
272@
C1386
10U 6.3V M X5R 0603 H0.8
C1387
0.1U_0402_16V4Z
U81
VDD
PVDD
PVDD
NC
SHUTDOWN#
EC_MUTE#
EC_MUTE# <28,31>
GAIN0
GAIN1
LOUT-
ROUT-
LOUT+
ROUT+
SPKL-
SPKR-
SPKL+
SPKR+
<28,30> AMP_LEFT
<28,30> AMP_RIGHT
C1388
0.47U_0603_10V7K
R1581
0_0402_5%
AMP_C_LEFT
C1389
R1582
AMP_C_RIGHT
C1390
0.47U_0603_10V7K
C1391
LIN-
RIN-
LIN+
RIN+
GND
BYPASS
C1392
0.47U_0603_10V7K
APA2031RI-TRL_TSSOP20
091109 change U81 symbol to
APA2031RI-TRL_TSSOP20
P/N: SA00001RZ00
Keep 10 mil width
Int. Speaker Conn.
20mil
<28> SPKL+
<28> SPKL-
<28> SPKR+
<28> SPKR-
R1577
R1578
R1579
R1580
0_0603_5%
SPK_L+
SPK_L-
SPK_R+
SPK_R-
JP25
G1
G2
ACES_88266-04001
CONN@
SPK_R-
SPK_R+
D51
PJDLC05C_SOT23-3
SPK_L-
SPK_L+
D52
PJDLC05C_SOT23-3
20081029 Update to 6dB
+5VAMP_J
R1586
100K_0402_5%
R1587
100K_0402_5%
GAIN0
GAIN1
R1589
100K_0402_5%
R1590
100K_0402_5%
272@
Headphone JACK
<28,30> HP_RIGHT
HP_RIGHT
271@
R1583
56.2_0402_1%
<28,30> HP_LEFT
HP_LEFT
R1584
56.2_0402_1%
HPOUT_L_1
L52
FBM-11-160808-700T_0603
HPOUT_L_2
<28,30> HP_RIGHT
R1585
56.2_0402_1%
HPOUT_R_1
L53
FBM-11-160808-700T_0603
HPOUT_R_2
<28,30> HP_LEFT
R1588
56.2_0402_1%
20mil
C1393
330P_0402_50V7K
C1394
330P_0402_50V7K
JHP1
<28> HP_PLUG#
HP_PLUG#
SHLD1
SINGA_2SJ2285-112252
CONN@
091123 change symbol of JHP1 to
SINGA_2SJ2285-112252
MIC1_VREFO
MIC1_VREFO
D53
RB751V-40TE17_SOD323-2
D54
RB751V-40TE17_SOD323-2
MIC1_VREFO_L
R1591
0_0402_5%
R1592
0_0402_5%
MIC1_VREFO_R
R1593
4.7K_0402_5%
R1594
4.7K_0402_5%
20mil
<28> MIC1_L
R1596
1K_0603_1%
MIC2_L_1
L55
FBM-11-160808-700T_0603
MIC2_L_2
<28> MIC1_R
R1595
1K_0603_1%
MIC2_R_1
L54
FBM-11-160808-700T_0603
MIC2_R_2
C1395
220P_0402_50V8J
C1396
220P_0402_50V8J
MIC JACK
JMIC1
<28> MIC_PLUG#
MIC_PLUG#
SHLD1
SINGA_2SJ2285-112252
CONN@
091123 change symbol of JMIC1 to
SINGA_2SJ2285-112252
EC Beep
<31> BEEP#
R1326
47K_0402_5%
MONO_IN_1
C812
0.1U_0402_16V4Z
MONO_IN
MONO_IN <28,30>
<19> SB_SPKR
R1327
47K_0402_5%
PCI Beep
R1328
4.7K_0402_5%
C811
0.1U_0402_16V4Z
091127 change value of R1328 from 10K to 4.7K
091020 follow NTV00 Design

Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

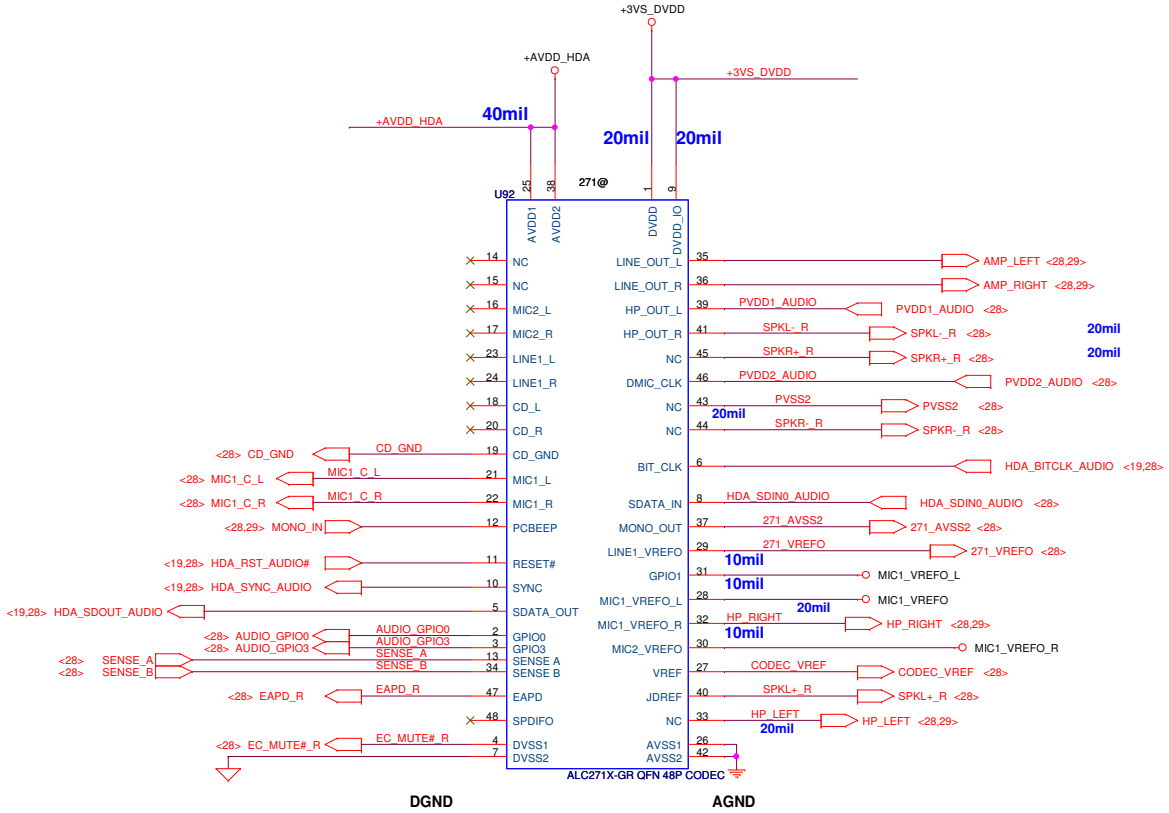
Compal Electronics, Inc.

Title: AMP & Audio Jack

Size: Custom | Document Number: NAVD0 LA-6091P | Rev 1.0

Date: Wednesday, March 03, 2010 |

HD Audio Codec



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

Compal Electronics, Inc.

Title: AUDIO CODEC ALC271

Size	Document Number	Rev
Custom	NAVD0 LA-6091P	1.0

Date: Wednesday, March 03, 2010 | Sheet 30 of 46

Change R1292 to 0 ohm for BRD ID R01 (EVT) 091015

091212 Add C65
to prevent switch noise

0118 Change R1292 200K P/N from SD028200300 to SD028200380
Change R1292 18K P/N from SD028180200 to SD028180280

091022 add output pin FAN_PWM

20100115 change R1292 to 33K for Pre-MP phase

BOARD ID Table

	VCC	3.3V				
	Ra	100K				
	ID	BRD ID	Rb	Vab-Min	Vab-Typ	Vab-Max
NAVD0	0	R01 (EVT)	0	0V	0V	0V
	1	R02 (DVT)	8.2K	0.216V	0.250V	0.289V
	2	R03 (PVT)	18K	0.436V	0.503V	0.538V
	3	R10A (MP)	33K	0.712V	0.819V	0.875V
NAVE0	4	R01 (EVT)	56K	1.036V	1.185V	1.264V
	5	R02 (DVT)	100K	1.453V	1.650V	1.759V
	6	R03 (PVT)	200K	1.935V	2.200V	2.341V
	7	R10A (MP)	NC	2.500V	3.3V	3.3V

091022 add VGAPWRGD on Pin85, 20100104 delete WWAN_LED# on pin 85

20100104 delete WLAN_LED# on pin 38

091022 add DGPU_PWRGD on Pin98

091212 Add C36
to prevent switch noise

091212 Add C22, C23, C24
to prevent switch noise

C22 near PR99

C23 near PR199

C24 near R800

Add 0 ohm R1309 06/08

Change BT_ON# from Pin98 to Pin108 06/24

091102 reserve C816 33P on TP_CLK
follow RF team review

20100104 delete WLAN_LED_R# on pin 16
20100104 delete WWAN_LED_R# on pin 19
091015 add HDMI_DETECT on Pin16
091026 add VGA_DEEP_IDLE on Pin17

0104 Delete WWAN_LED_R#, WLAN_LED_R#, WWAN_LED#, WLAN_LED#

100112 delete JP26 for EC debug port

091123 change SPI ROM to
SA00002TO00 (2MB)

16M SPI ROM

Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

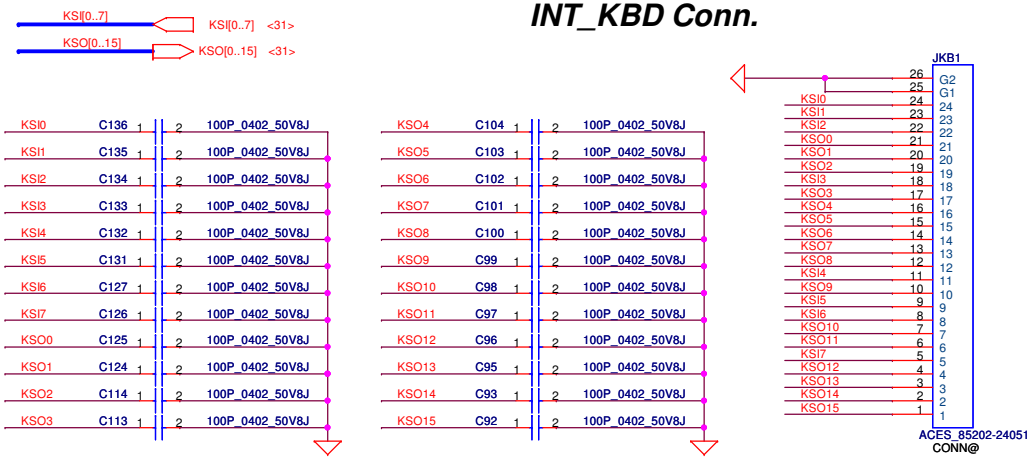
Compal Electronics, Inc.

Title: KB926/BIOS

Size: Custom | Document Number: NAVD0 LA-6091P | Rev: 1.0

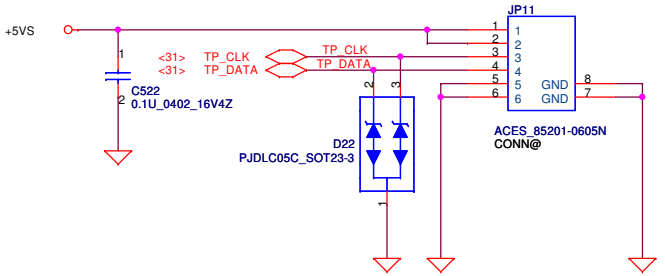
Date: Wednesday, March 03, 2010 | Sheet 31 of 46

INT_KBD Conn.



0108 Change 24 caps BOM structure from @ to mount (EMI)

To TP/B Conn.



Chage JP11 Pin define & Add D22 05/14

0111 Add C522 for JP11 pin1

Update TP/B Conn 05/04

Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

Compal Electronics, Inc.

Title: KB/SW/TP/LPC Debug CONN

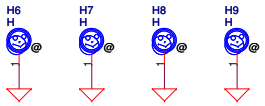
Size	Document Number	Rev
B	NAVD0 LA-6091P	1.0

Date: Wednesday, March 03, 2010 Sheet 32 of 46

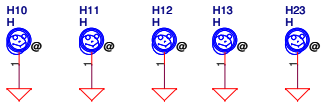
091028 Modify Hole location by 1127_NAVD0_NEW_MB_ASSY_FOR_2865_v11

H_3P2N

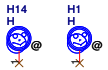
H_2P8



H_2P6



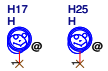
H_3P8N



H_8P7X5P8N

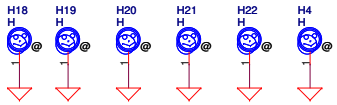
H_3P4X3P2N

H_3P0N



20100201 change H4 from H_3P2N to H_3P2

H_3P2



FIDUCIAL_C40M80

Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

Compal Electronics, Inc.

Title: Screw

Size	Document Number	Rev
B	NAVD0 LA-6091P	1.0

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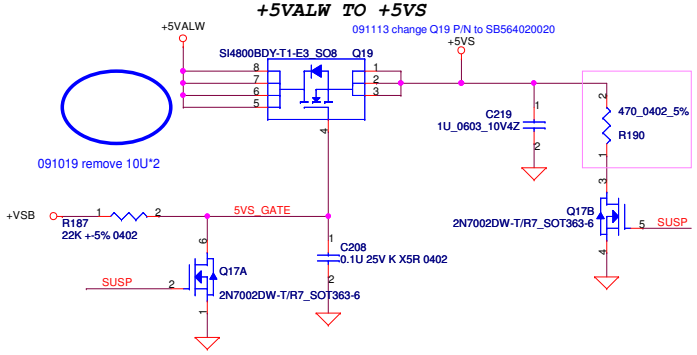
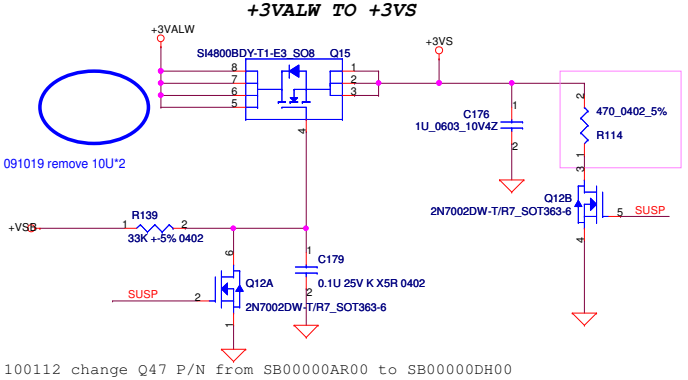
+5VALW TO +5VS



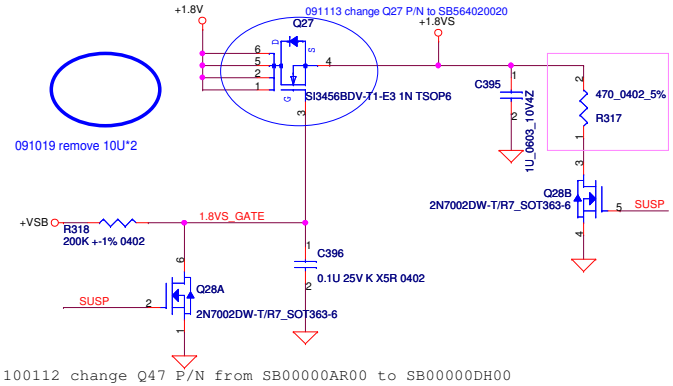
100112 change Q47 P/N from SB00000AR00 to SB00000DH00

+3VALW TO +3VS

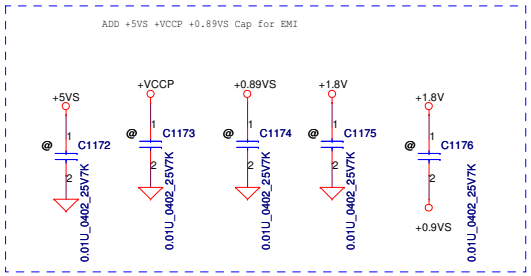


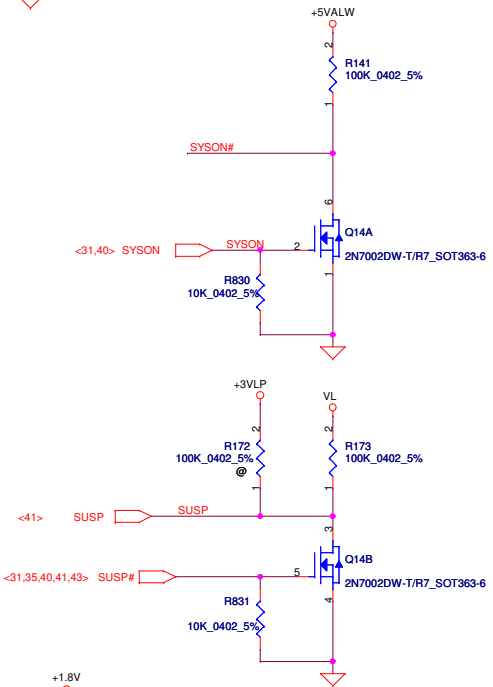
100112 change Q47 P/N from SB00000AR00 to SB00000DH00

+1.8V to +1.8VS

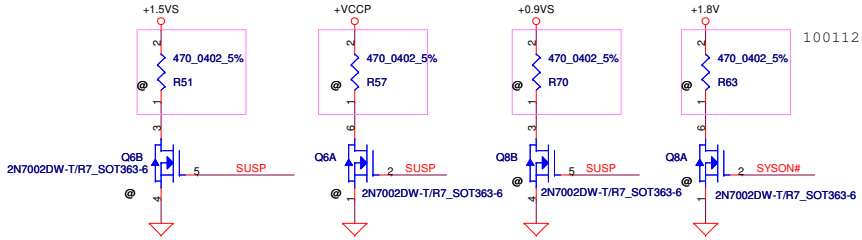


100112 change Q47 P/N from SB00000AR00 to SB00000DH00





100112 change Q47 P/N from SB00000AR00 to SB00000DH00



Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

Compal Electronics, Inc.

Title: DC INTERFACE

Size	Document Number	Rev
B	NAVD0 LA-6091P	1.0

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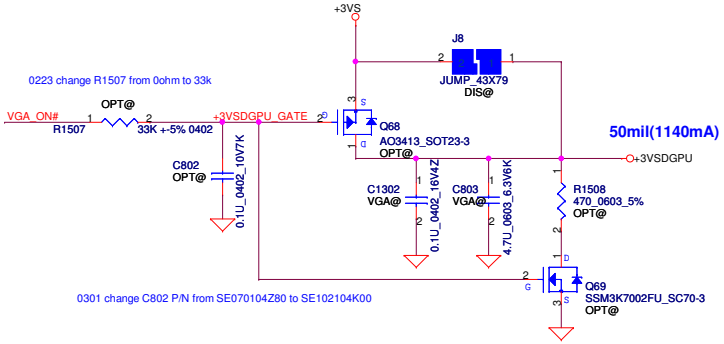
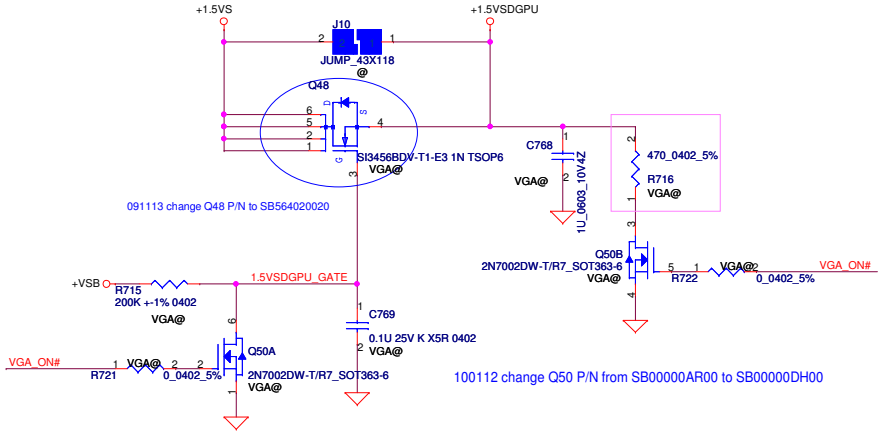
+3VS to +3VSDGPU Transfer

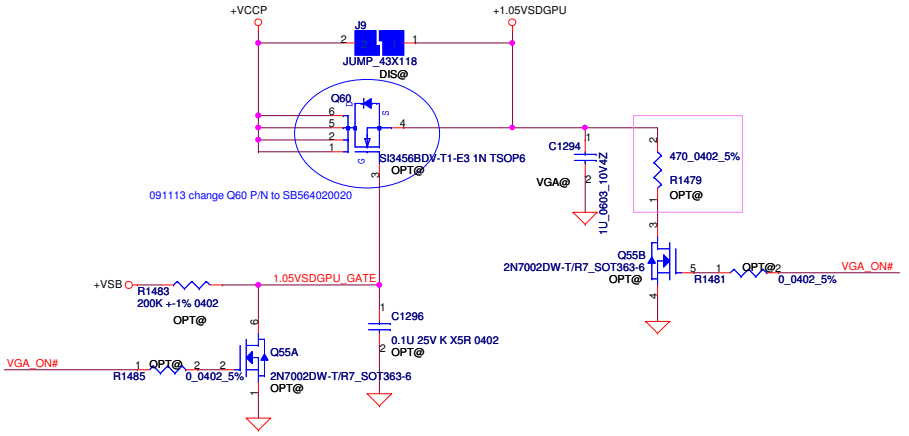
0111 Change BOM Structure of C1302/C803/C1303/C801/C1294 from OPT@ to VGA@



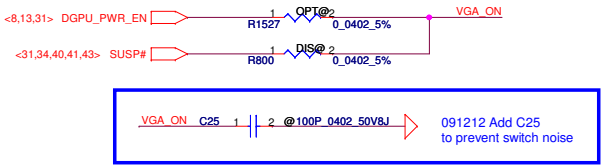
+1.5VS to +1.5VSDGPU Transfer



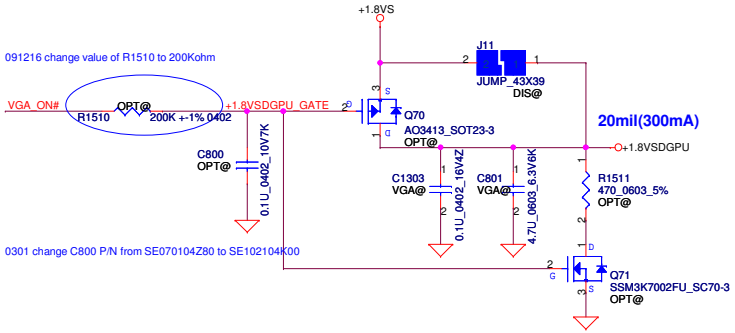
+VCCP to +1.05VSDGPU Transfer

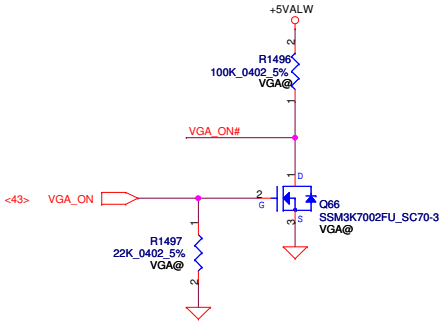


100112 change Q55 P/N from SB00000AR00 to SB00000DH00



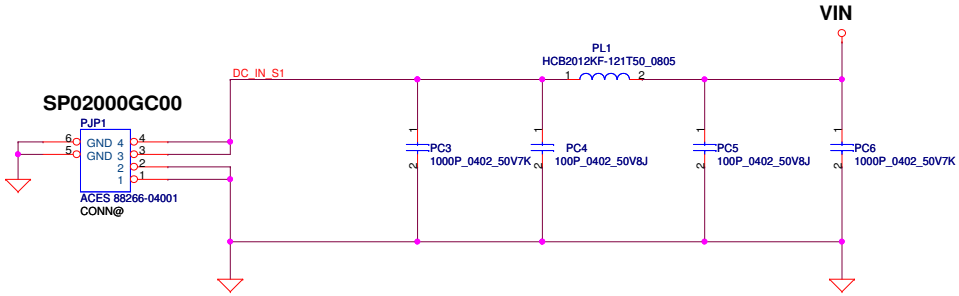
+1.8VS to +1.8VSDGPU Transfer

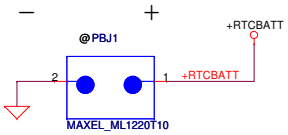


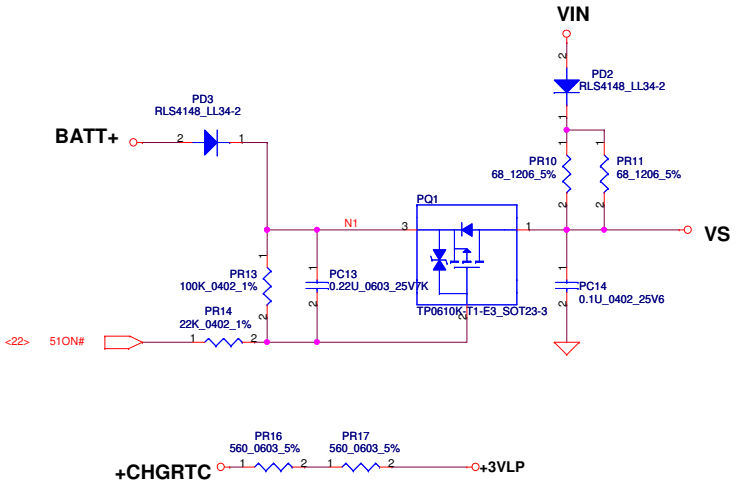


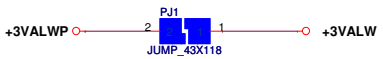
Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

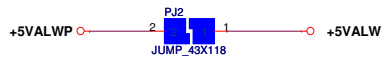
Compal Electronics, Inc.			
Title	VGA DC INTERFACE		
Size: Custom	Document Number: NAVD0 LA-6091P		Rev: 1.0
Date: Wednesday, March 03, 2010	Sheet 35 of 46		

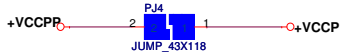


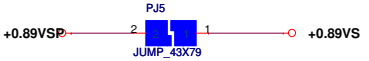












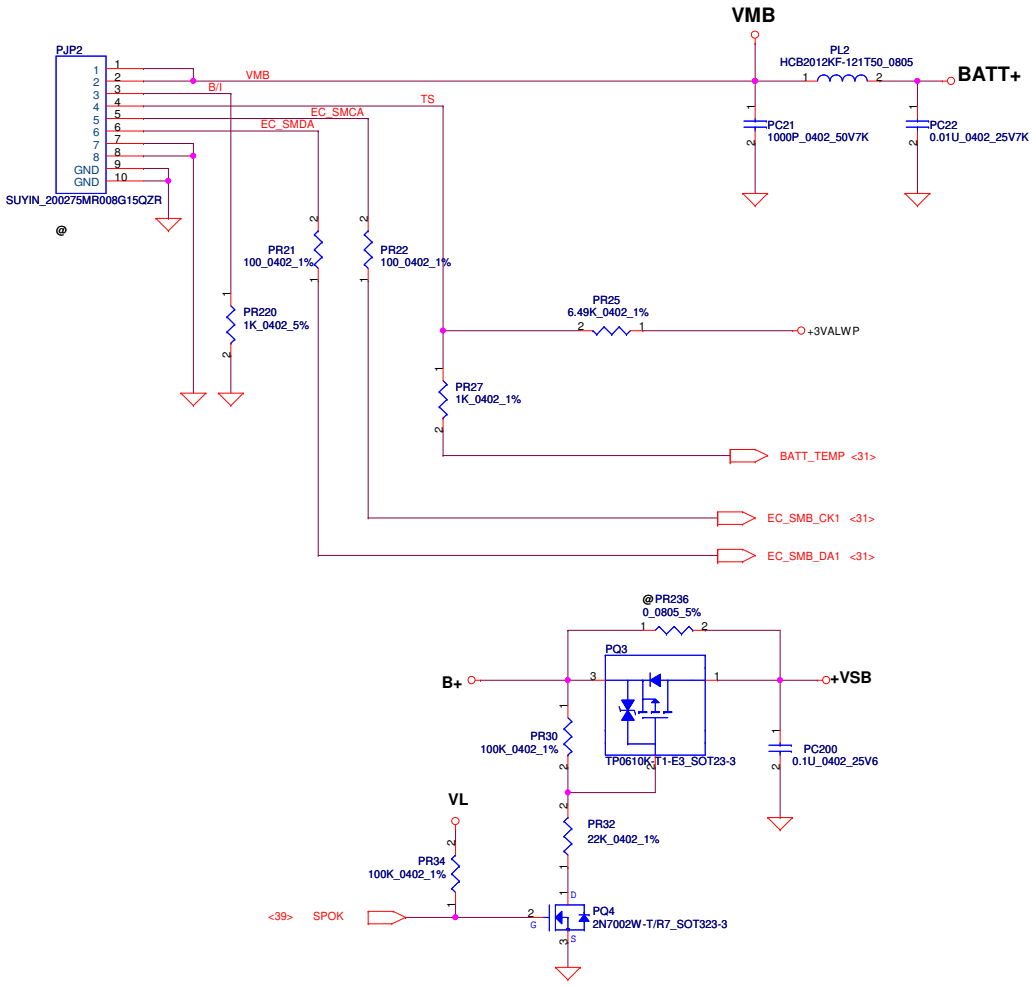
Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

Compal Electronics, Inc.

Title: DCIN/DECTOR

Size	Document Number	Rev
Custom	NAVD0 LA-6091P	1.0

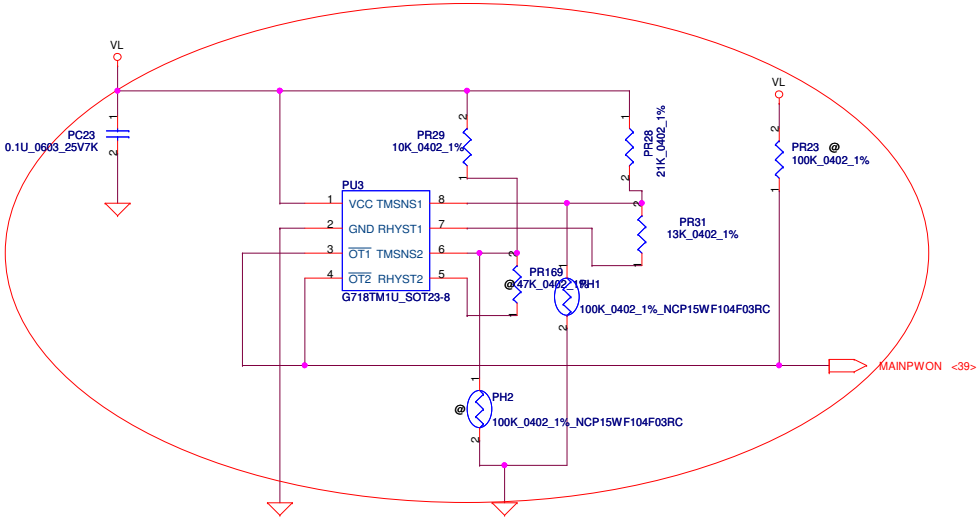
Date: Wednesday, March 03, 2010 | Sheet 36 of 46



PH1 under CPU botten side :

CPU thermal protection at 92 degree C

Recovery at 70 degree C



Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size: Custom | Document Number: NAVD0 LA-6091P | Rev: 1.0

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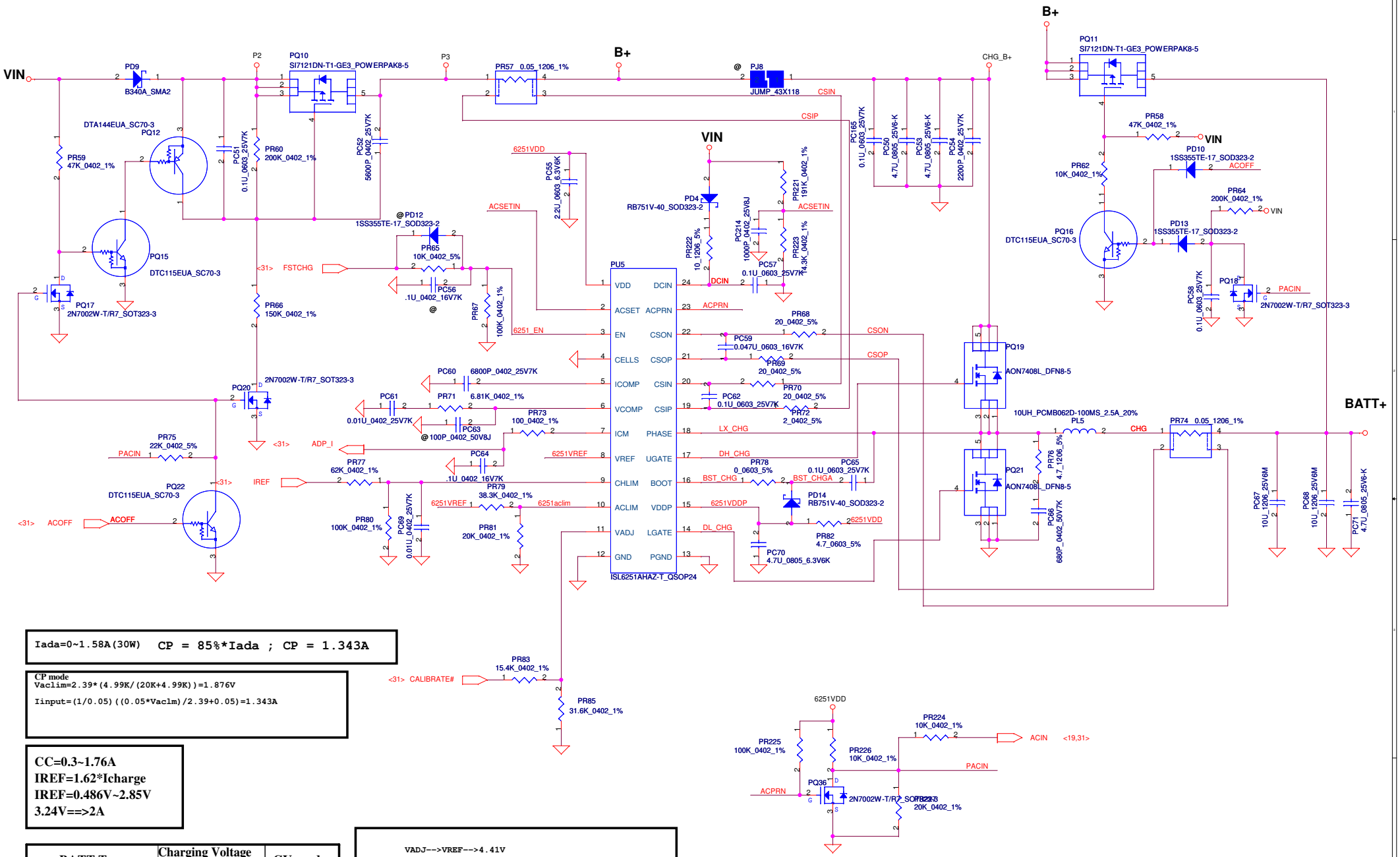

Iada=0~1.58A(30W) CP = 85%*Iada ; CP = 1.343A

CP mode
Vaclim=2.39*(4.99K/(20K+4.99K))=1.876V

Iinput=(1/0.05)((0.05*Vaclm)/2.39+0.05)=1.343A

CC=0.3~1.76A
IREF=1.62*Icharge
IREF=0.486V~2.85V
3.24V==>2A

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

VADJ-->VREF-->4.41V

VADJ--->Ground--->3.99V

Vcell=(0.175*VADJ+3.99)

Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

Compal Electronics, Inc.

Title: CHARGER

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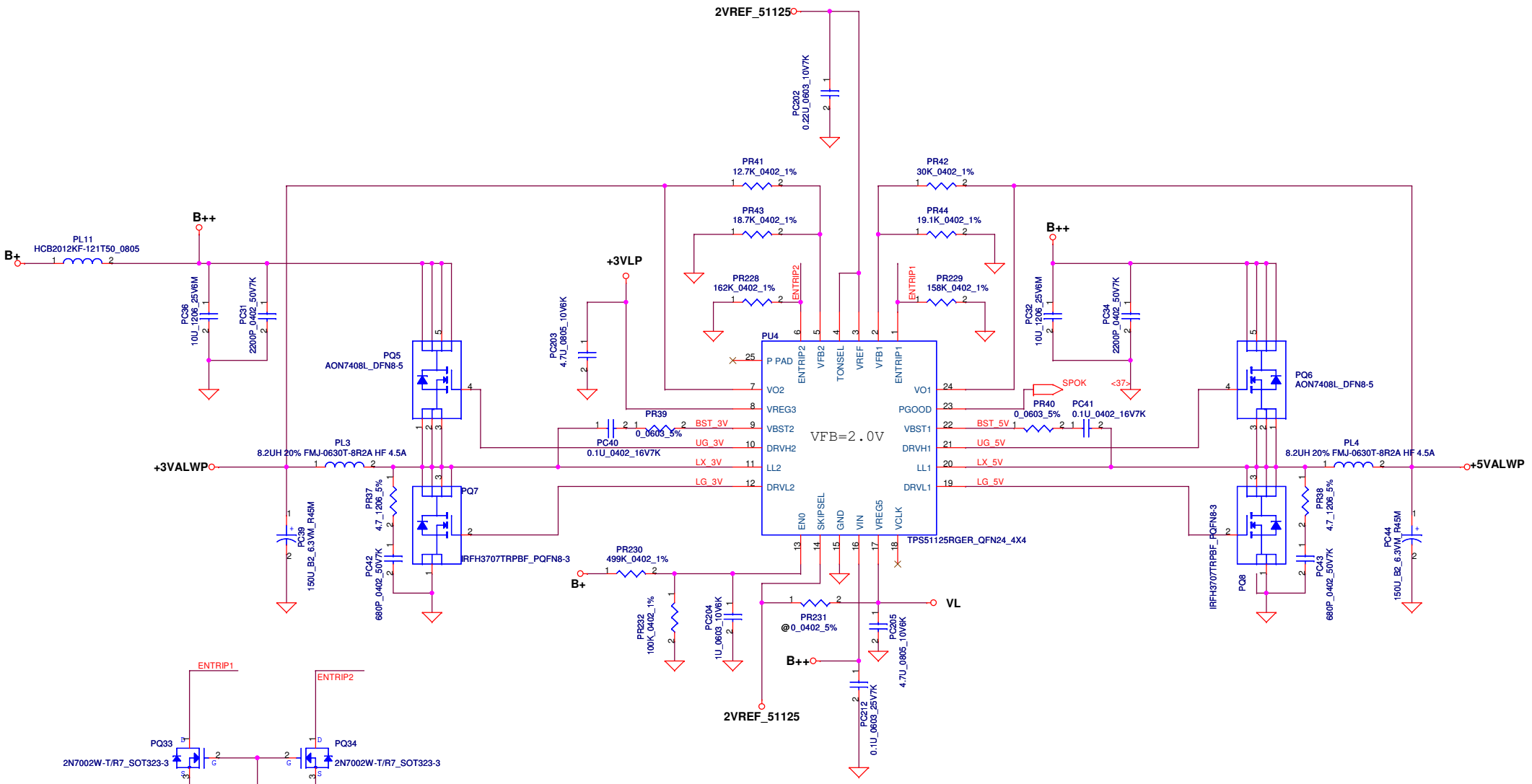

+3.3VALWP Ipeak=6.42A=(5.82+0.6)A Imax=4.5A Vo=3.3V
Rds(on)=17.9m ohm(max) ; Rds(on)=14.5m ohm(typical)
Vtrip=(10E-06 * 143K)/9-24mV=156mV
Ilimit=156/(14.5~14.5*1.2)=10.76~7.26 A

Iocp=Ilimit+Delta I/2
=11.3~7.81A
Delta I=1.090A (Freq=305KHz)

+5VALWP Ipeak=3.86A Imax=2.7A Vo=5.14v
Rds(on)=17.9m ohm(max) ; Rds(on)=14.5m ohm(typical)
Vtrip=(10E-06 * 158K)/9-24mV=151mV
Ilimit=151mV/17.9m ~151mV/14.5m x 1.2
=8.467A ~ 8.710A
Iocp=Ilimit+Delta I/2
=9.384A ~ 9.627A
Delta I=1.834A (Freq=245KHz)

Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

Compal Electronics, Inc.

Title: 3V/5V

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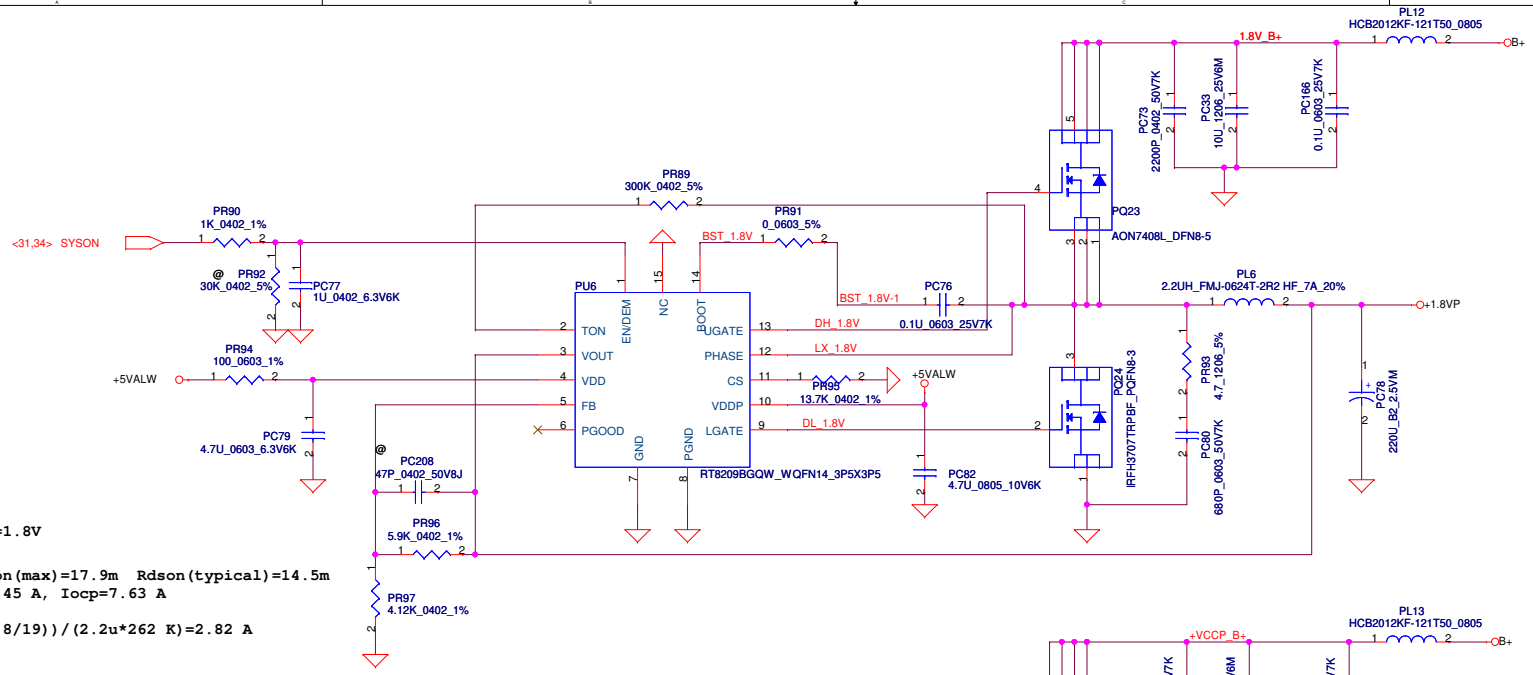
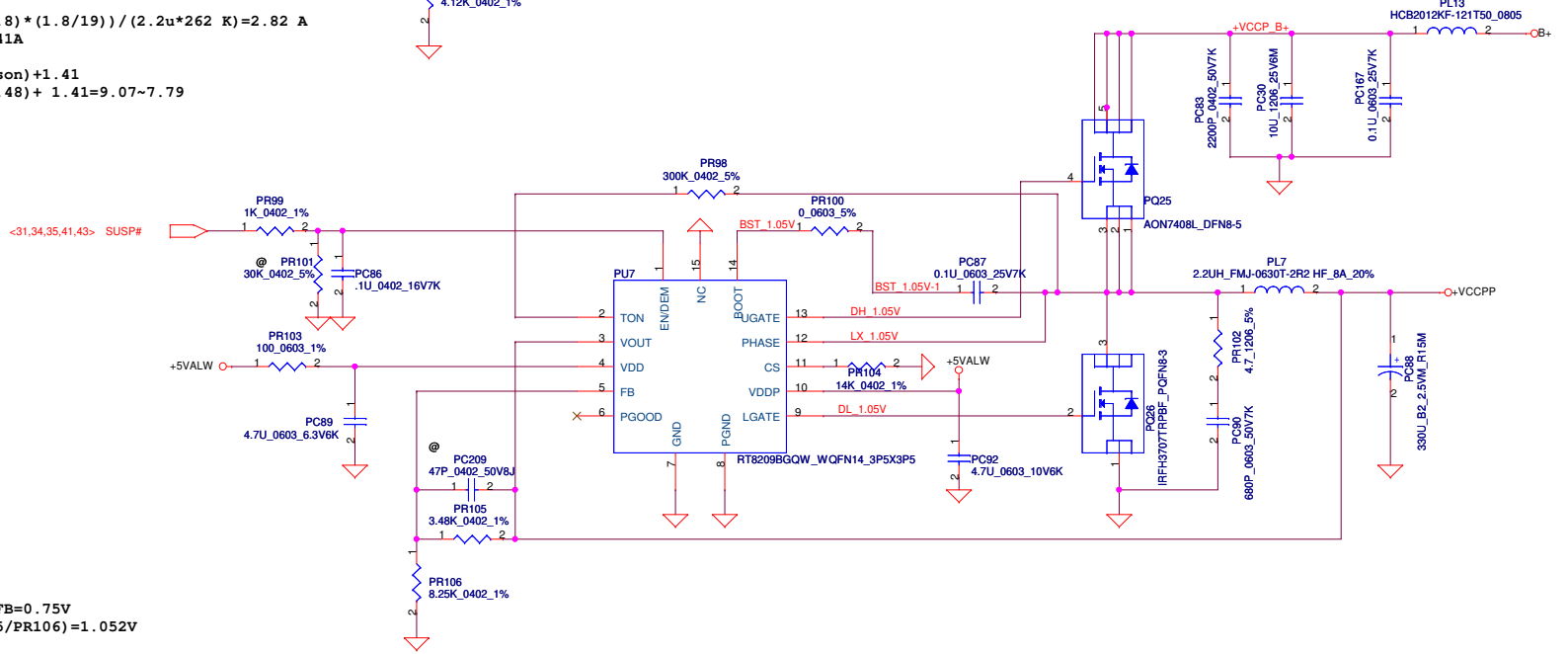


<Vo=1.8V> VFB=0.75V
Vo=VFB*(1+PR96/PR97)=1.8V
Fsw=262 KHz

Cout ESR=15m ohm Rdson(max)=17.9m Rdson(typical)=14.5m
Ipeak=6.36 A, Imax=4.45 A, Iocp=7.63 A

Delta I=((19-1.8)*(1.8/19))/(2.2u*262 K)=2.82 A
=>1/2DeltaI=1.41A
Vtrip=137mV
Iocp=Vtrip/(Rdson)+1.41
=95.3/(17.9~21.48)+ 1.41=9.07~7.79



<Vo=1.052V> VFB=0.75V
Vo=VFB*(1+PR105/PR106)=1.052V
Fsw=262KHz

Cout ESR=15m ohm Rdson(max)=17.9m Rdson(typical)=14.5m
Ipeak=6.1A, Imax=4.27 A, Iocp=7.32 A
Delta I=((19-1.05)*(1.05/19))/(2.2u*262K)= 1.72A
=>1/2DeltaI=0.86A
Vtrip=14K*10uA=0.140 V

Iocp=Vtrip/(Rdson)+0.86
=113/(17.9~21.48)+0.86=8.68~7.37 A

Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

Compal Electronics, Inc.

Title: VCCPP/1.8VP

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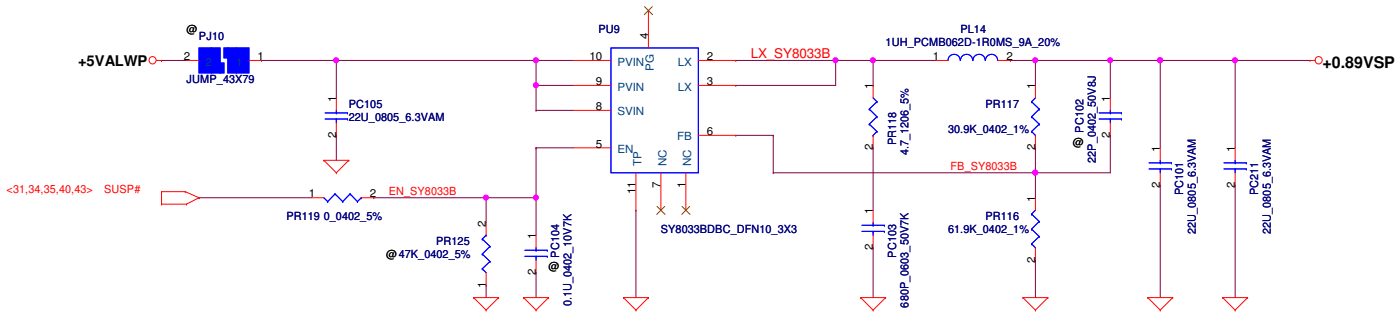
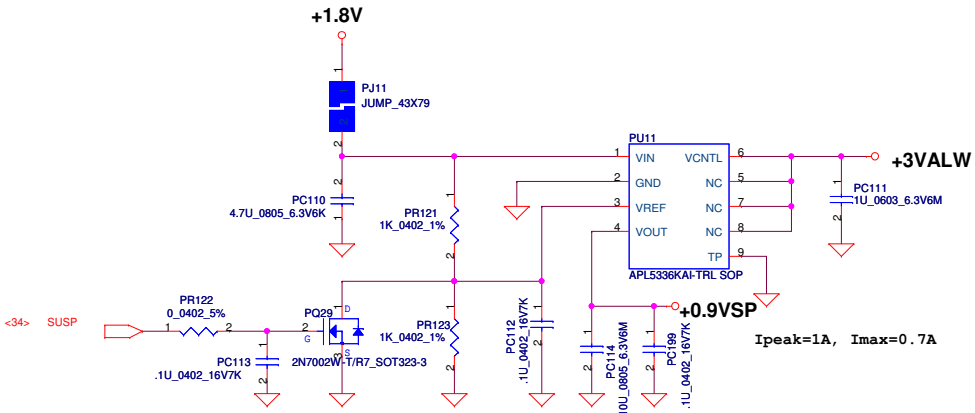
<Vo=0.89V> VFB=0.6V
Vo=VFB*(1+PR117/PR116)=0.6*(1+30.1K/61.9K)=0.8917V

Ipeak=2.64A





Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

Compal Electronics, Inc.			
Title	0.89VSP/0.9VSP		
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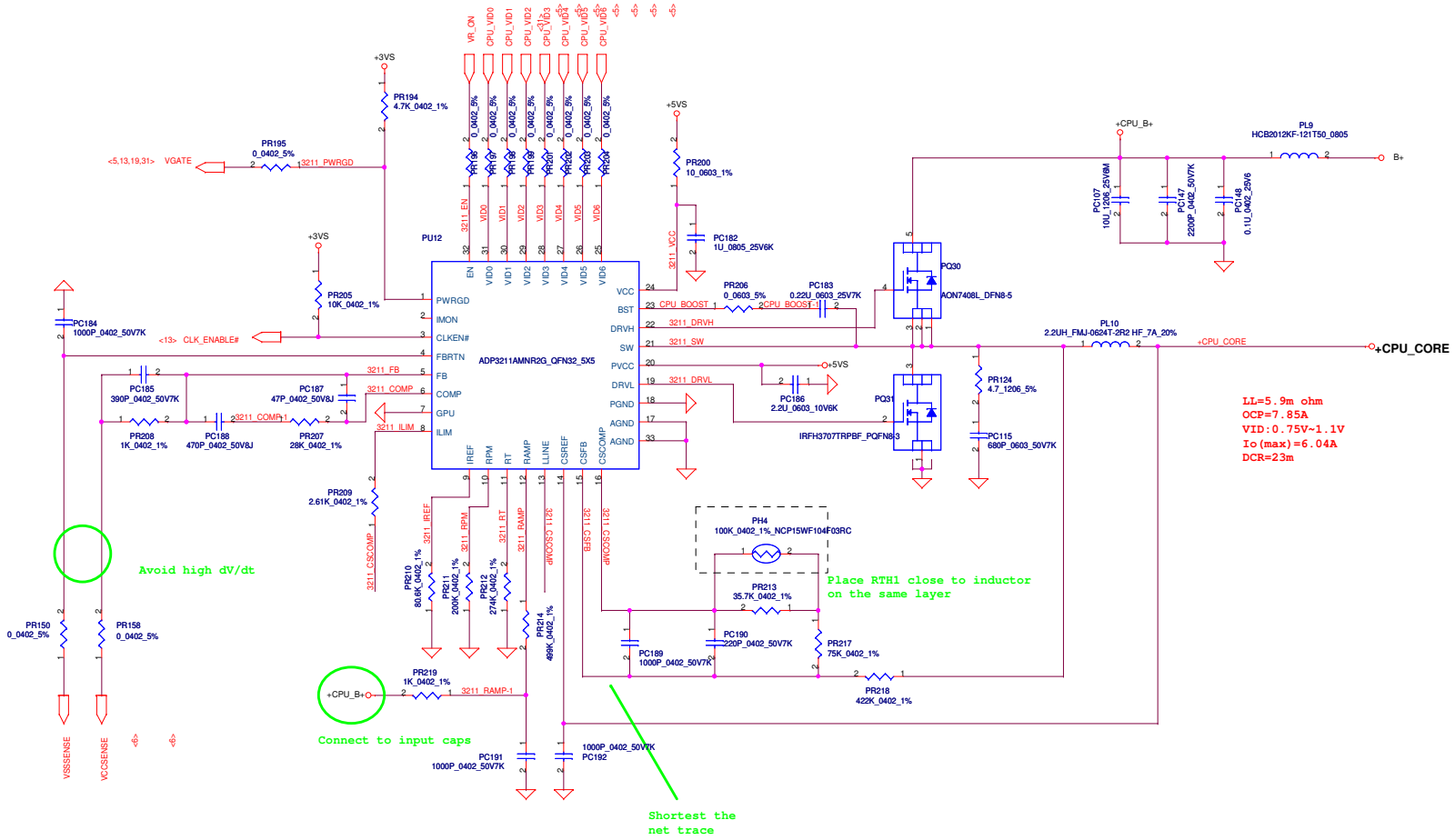

Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

Compal Electronics, Inc.

Title	CPU_CORE	
Size C	Document Number NAVD0 LA-6091P	Rev 1.0
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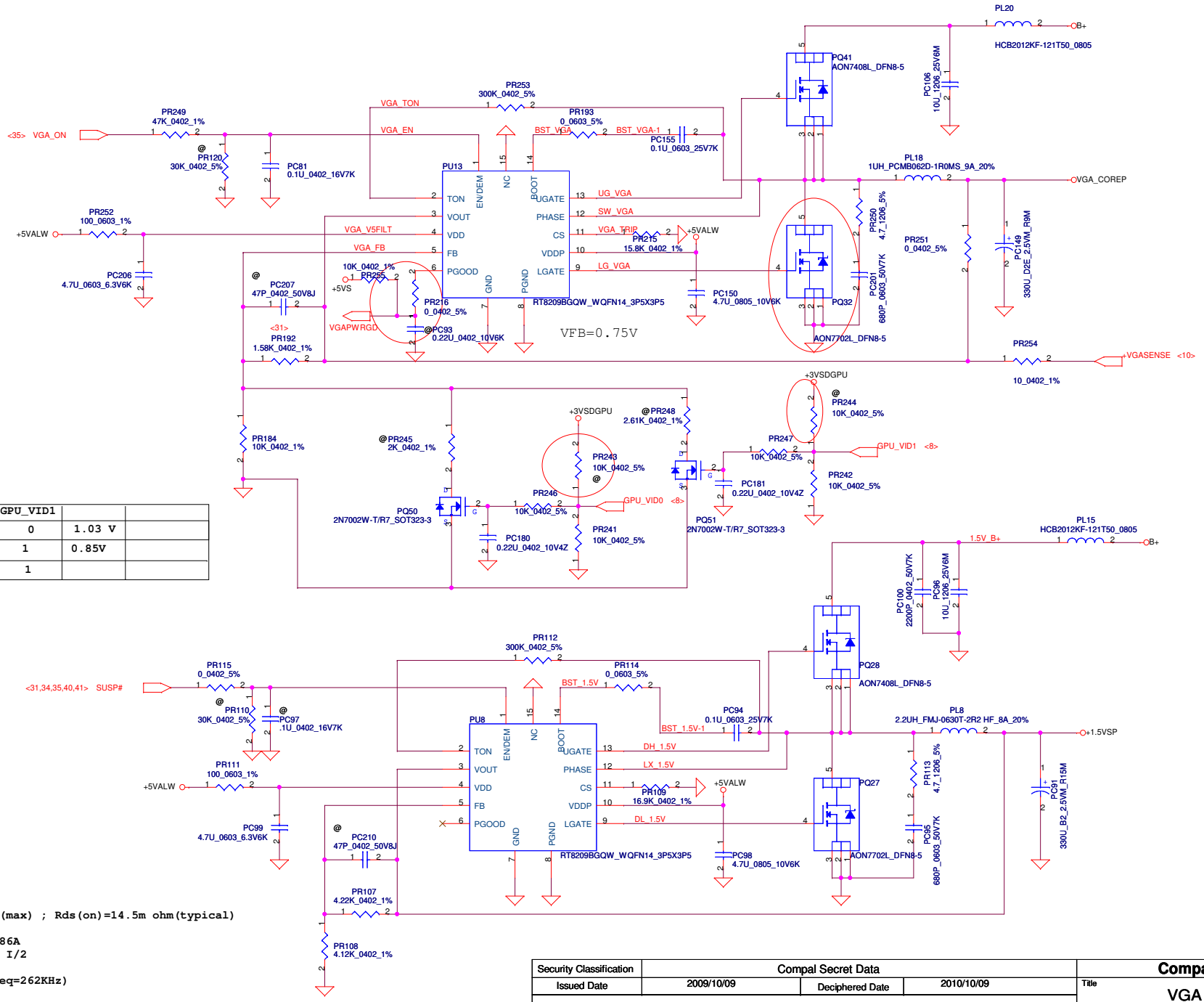
Ipeak=11.6 A
Imax=8.15 A

delta I=3.27A 1/2 delta I=1.636 A
Iocp=RTEIP*ITRIP/RDS(ON)+1/2 I=14~11.98 A
Rds(on)=11~14m



GPU_VID0	GPU_VID1		
0	0	1.03 V	
0	1	0.85V	
1	1		

Vo=1.518V
Fsw=262 KHz

Ipeak=8.62 A
Imax=6.034 A
Iocp=10.35 A

Rds(on)=17.9m ohm(max) ; Rds(on)=14.5m ohm(typical)

Ilimit=9.44A ~ 7.86A
Iocp=Ilimit+Delta I/2
=12~10.5A
Delta I=5.27A (Freq=262KHz)

Security Classification	Compal Secret Data		
Issued Date	2009/10/09	Deciphered Date	2010/10/09

Compal Electronics, Inc.		
Title	VGA_CORE/1.5VSP	
Size: Custom	Document Number: NAVD0 LA-6091P	Rev: 1.0
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For save layout space and shortage	A		change PC50 PC53 to 0805 4.7u		
2		For VGA_core 51117 power good delay	A		Reserve PR216 PC93		
3		Save layout space	A		Delet PC35 PC36, change PC29 PC32 to 1206 10uF		
4		For cost down	A		change 0.89V from MP2121 to SY8033		
5		For cost down	A		delet Vin detector,battery OVP circuit		
6		For cost down	A		change 3V/5v from ISL6237 to TPS51125		
7		For Design change	A		change PR116 to 61.9K PR117 to 30.1K PL14 to 1uH		
8		For cost down	A		change 1.5V PL8 to 3mm height		
9		For cost down	A		change VCCP PL7 to 3mm height		
10		For Design change	A		change PQ31 to IRFH3707		
11		For Design change	A		change PQ23 PQ25 PQ28 PQ30 TO AON7408		
12		change 1.5V enable RC ,for HW request	A		change PR115 to 0 ohm ,unpop PR101		
13		change VCCP enable RC ,for HW request	A		change PR99 to 1k ohm ,pc86 to 0.1u,unpop PR110		
14		change VGACORE enable RC ,for HW request	A		change PR249 to 47k ohm ,pc81 to 0.1u,unpop PR120		
15		For charger ripple			Add PC71 4.7u 0805 25V		
16		For charger ripple			change PL5 to 10uF		
17		Buyer suggest			change PQ36 from 2N7002 TO SSM3K7002FU		
18		Fix VGA_VID at 0.85V			delete PR248 PR245 ,change PR192 to 1.58K		
19		OTP INPUT PULL HIGH resister			Add PR29		
20		change OTP set			change PR31 to 13K		
21		1.8V enable cap			Add PC77 1u 6.3v X5R		
22		51125 VL cap size up to 1206			change PC205 to 1206 size		
23		Buyer suggest			change PC96 PC106 PC107 from X6S to X5R		

Compal Electronics, Inc.
Title: PIR-PWR-1
Size: Custom Document Number: NAVD0 LA-6091P Rev: 1.0
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1						2009.6.30	EVT
2						2009.6.30	EVT
3						2009.7.2	EVT
4						2009.8.4	EVT
5						2009.8.12	EVT
6						2009.8.12	EVT
7						2009.8.12	EVT
8						2009.8.12	EVT
9						2009.8.24	EVT
10						2009.8.24	EVT
11						2009.8.24	EVT
12						2009.8.24	EVT
13						2009.8.24	EVT
14						2009.8.24	EVT
15						2009.8.27	EVT
16						2009.9.4	DVT
17						2009.9.10	DVT
18						2009.9.30	PVT
19							
20							
21							
22							
23							

Compal Electronics, Inc.

Title: PIR-PWR-2

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<2009/4/28>
Update new power schematic,
release first version NAV50 schematic

<2009/04/29>
. Add R1182 R1183 L3 on page 9
. Change J3 to R1184 on page 13

<2009/04/30>
. Change JDIM1 to SP07F001720 on page 7
. Del SATA1 Port on page 12
. Change R51 R57 R70 R63 R317 R314 R190 to 0402 Size on page 21

<2009/05/04>
. Add WWAN_CLKREQ# and R107 pull-high to +3VS on page 8
. Add CRT_DET# on page 10
. Add CRT_DET# circuit on page 13
. Add 3 LEDS on page 16
. Add BT/BTN Board CONN. on page 16
. Update TP/B CONN. to SP01000LB00 on page 19

<2009/05/11>
. Add INVT_PWM on Page 5
. Del R323 on page 5
. C74 change to 2.2U_0603 on page 6
. C267 change to 22U on page 6
. C391 change to 0.1U on page 6
. Del C67 C35 C33 C36 on page 6
. Del +LGI_VID and U71.A21 direct connect to +VCCP on page 6
. Follow Intel checklist, add R52 on FSB on page 8
. Add D5 D7 D8 on page 4
. Add R174 on page 9
. Add PCI_RST# on page 11
. Add C1115 C1114 C1116 C1117 C1118 on page 15

<2009/05/12>
. Follow Intel Layout Checklist, Add C141 on VDDSPD on page 7
. Modify SRC CLK PORT LIST on page 8
. Del CLKREQ_LAN# on page 8
. Change PCIE Port list on page 13
. Change USB Port list on page 13
. Add W/L 3G SW on page 16
. Del R103 on page 18

<2009/05/13>
. Change JMINI1 to PCIE Port 3 on page 15
<2009/05/14>
. Page8 Change C174 C175 to 10U_0603

<2009/05/14>
. Update New Power schematic
. Del R376 R377 on page 8
. Del D5 D7 D8 on page 4
. Change JLVDS1 to SP010006810 on page 9
. Add D6 for EMI on page 9
. Change C1106 to C_0603 type on page 9
. Change USB_OC# on page 13
. Add USB Port2 on page 20
. Change JP11 Pin define & Add D22 on page 19
. Change C512 to 1u_0402 on page 15
. Add U29 (MEDIA_LED#)) on page 16

<2009/05/19>
.Update new clock GEN co-lay schematic on page 8

<2009/06/05>
.Update new clock GEN co-lay schematic on page 8
.Follow Intel check list change C161 C165 to 27P on page 8
.Follow Intel check list change C56 to 22uF on page 6

<2009/06/08>
.Update New Power schematic 06/06 version
Page 13- a.Del R203 (pull-up GPIO6 Resister)
b.Change R1184 NU
Page 17- a. Add VGATE
b. Del R1294
c. Change D30 NU
d. Change R1295 to 0 ohm
e. Add R1309 0 ohm on EC_RSMRST#
f. Pull-up LAN_WAKE# +3VALW
g. ICH_POK change to PCH_POK
h. Pull-up KB_RST# to +3VS
Page 10- a. Add R1283 R1284 ,Change R247 R249 to 10 ohm
b. Add @ on U10 U11 C301 C298
c. Del C302 C300 R1281 R1287

<2009/06/10>
. Page 7- Add C116 @
. Page 22- Modify USB_OC#1_2 to USB_OC#2
. Page 17- Modify PLTRST# to PCI_RST#
. Page 17- Add @ on R1311

<2009/06/12>
. Page4 Add C314 C313 C1150 D19 on +VCC_FAN1
. Page8 Add C1145 C1146 C1147
. Page10 Move CRT_DET# from Page13 to Page10
. Page13 Add +RTCVCC circuit

<2009/06/15>
. Update New Power schematic (change PBJ1 to PJP3)
. Page 10 modify C310 C308 C303 C307 C306 C304 Bom Structure
. Page 22 Modify Hole location by (ME drawing 06/12)

<2009/06/16>
. Page7 Modify DDR Command Control Pin pull-high Resister location
. Page9 Change R577 to 0402 type

<2009/06/17>
. Update New Power schematic 06/17
. Page9 modify LVDS Conn. Pin define
. Page9 Del C1110
. Page4 Add EMI solution D38 D39 D40

<2009/06/18>
. Update New Power schematic 06/18
. Page8 modify U4 Pin define and Q31
. Page13 Add R1376, R1377
. Page15 Modify C403
. Page23 Modify H11

<2009/06/19>
. Page4 Add new signal CPU_ITP , CPU_ITP#
. Page5 ADD R1378
. Page6 ADD C1152,C1153,C1154 C1160,C1161,C1162
. Page7 DDR_A_D8與DDR_A_D9互換
. Page8 ADD R1379,R1380,U77,R1381,C1157,R1382,R1383,R1384,C1157
, Page8 DEL C390
. Page9 ADD C1156
. Page11 DEL R1322, R1154
. Page13 DEL U77, ADD C1158
. Page17 ADD C1159

<2009/06/22>
. Page22 change IO Conn. pin34 from 48M to USB_ON#
. Page10 change JCRT1 P/N to SP010906182

<2009/06/23>
. Page15 Add C1163 C1164 C1165 C1166
. Page18 change PWR/B Conn. P/N to SP01000H300
. Page22 change JUSB1 JUSB2 P/N

<2009/06/24>
. Page8 Change C1350 C1351 to 0402 type
. Page10 Add R1385 R1386 on JVGA_HS JVGA_VS

<2009/06/25>
. Page22 move some parts to I/O Board , Add the MONO_IN_R on M/B
.
<2009/06/29>
. Page16 Change JP24 to ACES_88266_05001
. Page15 Change JMINI1 to FOX_AS0B246-S50U-7F_52P-T

<2009/06/30>
. Page18 Change PWR_LED# to PWR_PWM_LED#
. Page17 Add PWR LED DETECT PIN on Pin97

<2009/07/02>
. Update New Power schematic 07/02
. Page9 Add C1167 C1168 for RF request.
. Page13 Change R223 to 100K
. Page16 change JP24 to ACES_85201-0505N
. Page17 Del R1387 R1388 on EC Pin97
. Page17 Add New Board ID to separate NAV50 NAV60
. Page17 Change 展頻IC to SA00003J400 (New)
. Page18 Add D41 for ESD

<2009/07/03>
. Page18 Add D41.2 to PWR_PWM_LED#
. Page8 Change co-lay net name to +1.5VM_CK505
. Page20 Change JP2 Pin42 to +5VS

<2009/07/06>
. Page18 Add pwr switch for NAV50

<2009/07/08>
. Page5 Add 470pf on H_SMI# for known issue.

<DVT START>

<2009/08/04>
. Page5 CLK_CPU_HPLCLK CLK_CPU_HPLCLK# exchange
. Page9 Change JLVDS1 to P/N ACES 88341-3001 30P
. Page17 del PM_1.8V(U6.82) ,Del R1310 R1311
. Page18 Del D41

<2009/09/03>
. Page7 Change C112 to 0402 type
. Page8 Add T6 on CLK_48M_CR
. Page16 Modify JP18 Pin define change +5VALW +5VS to +3VALW +3VS
. Page20 Change Pin 18, 23 to +1.5VS change Pin7 , 9 to USB20_P7 N7
. Page21 Del H12

<2009/09/08>
Update Power schematic 0904
. Page18 Change R1388 to 100 ohm 0402
. Page18 Change LED1 to SC591NB5A00

<2009/09/10>
Update Power schematic 0910
. Page22 unmount Q6 Q8

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: PIR -HW

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